TM 11-6625-2578-34

TECHNICAL MANUAL

DIRECT SUPPORT AND GENERAL SUPPORT

MAINTENANCE MANUAL

# RADIO TEST SET GROUP OQ-60/USQ-46

HEADQUARTERS, DEPARTMENT OF THE ARMY

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# Direct Support and General Support Maintenance Manual
# RADIO TEST SET GROUP OQ-60/USQ-46

## LIST OF ILLUSTRATIONS

LIST OF TABLES

# CHAPTER 1

# INTRODUCTION

## Section I.

### 1-1. Scope

*a.* This manual covers direct support and general support maintenance for the Radio Test Set Group OQ-60 USQ-16. Included is a functional description of the radio test set group, with troubleshooting, repair, replacement, adjustment alinement, and testing instructions for all required maintenance procedures. Also listed are tools, materials, and test equipment required for direct support, and general support maintenance

*b.* Operation, installation, and organizational maintenance instructions are in TM 11-6625-2578-12 which also contains the basic issue items listed and the maintenance allocation chart.

### 1-2. Maintenance Forms and Records

Department of the Army forms and procedures used for equipment maintenance will be those prescribed by TM 38-750.

### 1-3. Destruction of Army Material to Prevent Enemy Use

Destruction of this equipment will be accomplished in accordance with TM 750-244-2. Authorization to destroy this equipment must be given by divisional (or higher) commanders or a subordinate commander who has been delegated this authority. Destruction of the equipment will be reported through command channel

### 1-4. Administrative Storage

Administrative storage of this equipment shall be accomplished in accordance with instructions contained in TM 740-90-1.

### 1-5. Calibration

Pertinent publications on calibration of this equipment shall be referenced.

### 1-6. Reporting of Equipment Manual Improvements

The reporting of errors, omissions, and recommendations for improving this publication by the individual user is encouraged Reports should be submitted on DA Form 2028 (Recommended Changes to Publications) and forwarded direct to Commander, US Army Electronics Command, ATTN: AMSEL-MA-SR, Fort Monmouth, N J 07703.

## Section II. DESCRIPTION AND DATA

### 1-7. Description

Refer to TM 11-6625-2578-12 for the general description of the Radio Test Set Group OQ-60 USQ-46

### 1-8. General Characteristics

*a.* Refer to TM 11-6625-2578-12 for technical characteristic data for the Radio Test Set Group OQ-60 USQ-46.

*b.* In addition to the data listed in TM 11-6625-2578-12, reference designators, nomenclature, and common names of major assemblies and subassemblies of the radio test set group are provided in chart 1-1. The reference designators were assigned to the OQ-60/USQ-16 in accordance with the unit numbering method of American Standard, Electrical Reference Designation-ASA Y32.16.

*c.* The major assemblies or subassemblies are referred to by their common name throughout this manual

Chart 1-1. Radio Test Set Group OQ-60 USQ-46 Reference Designator, Nomenclature, and Common Name

| Reference designator | Nomenclature | Common name |
|---|---|---|
| 1 | Radio Test Set TS-2965 USQ-46 | Test set |
| 1A1 | Front panel module assembly | Front panel module assy |
| 1A1A1 | Voltage controlled crystal oscillator module assembly | VCXO |
| 1A1A2 | RF detector—output module assembly | RF detector |
| 1A1A3 | Loop filter—module assembly | Loop filter |
| 1A1A4 | Synthesizer mixer module assembly | Synthesizer mixer |
| 1A1A5 | Programable divider module assembly | Programable divider |
| 1A1A6 | Mode control I module assembly | Mode control I |
| 1A1A7 | RF mixer amplifier module assembly | RF mixer amplifier |
| 1A1A8 | Mode control II module assembly | Mode control II |
| 1A1A9 | Word length generator module assembly | Word length generator |
| 1A1A10 | Reference generator module assembly | Reference generator |
| 1A1A11 | Mode control III module assembly | Mode control III |
| 1A1A12 | Encoder I module assembly | Encoder I |
| 1A1A13 | Encoder matrix module assembly | Encoder matrix |
| 1A1A14 | Encoder II module assembly | Encoder II |
| 1A1A15 | Shift register module assembly | Shift register |
| 1A1A16 | Temperature compensated crystal oscillator | TCXO |
| 1A1A17 | Power supply regulator power assembly | Power regulator |
| 1A1A18 | Front panel assembly | Front panel assembly |
| 1W1 | RF Cable Assembly CG-3628 U | RF cable |
| 2 | Power Supply PP-6446A USQ-46 | Power supply |
| 2W1 | Ac Power Cable Assembly CX-12313 U | Ac cable |

# CHAPTER 2

# FUNCTIONING OF EQUIPMENT

## Section I. INTRODUCTION

### 2-1. General

The Radio Test Set TS–2963/USQ–46 with associated Power Supply PP–6446A/USQ–46 form a portable signal generating device designed to simulate all signals that RF Monitor Sets AN/USQ–46 or AN/USQ–46A can receive and act upon. The Radio Test Set generates fm signals from 160 to 176 MHz, providing 2520 output channels with 6.25 kHz channel spacing.

### 2-2. Functional Divisions

The radio test set consists of six functional sections as shown in figure 2–1. Paragraphs 2–6 through 2–12 describe the general functioning of each module within these sections. Detailed description of each module function is provided in paragraphs 2–13 through 2–16.

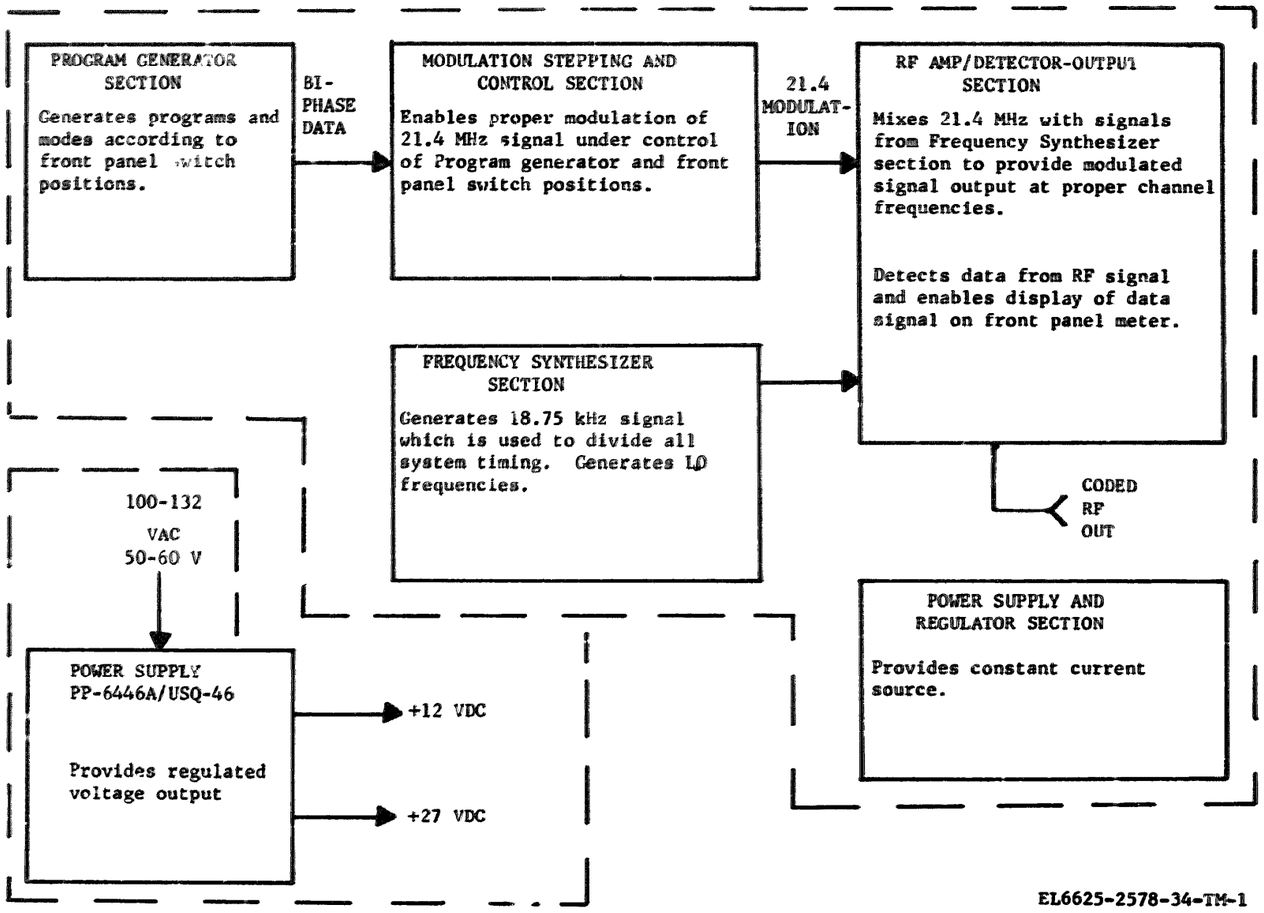



Figure 2-1. Radio test set basic block diagram.

## Section II. ANALYSIS OF RECURRING AND NONRECURRING INTEGRATED CIRCUITS

### 2-3. General

*a.* Integrated circuits (IC's) are used throughout the radio test set functional sections and almost entirely in the logic section. Each IC contains one or more logic elements such as NOR gates, inverters, flip-flops, shift registers, counters, or amplifiers contained in a protective package. Five package configurations are used throughout the Radio Test Set. These configurations are shown in figure 2–2 as an aid to pin number identification of various IC's.

*b.* The 14-pin flat packages (D and E, fig. 2–2) have a lead identification or manufacturers trademark dot in the upper left-hand corner which represents the pin number starting point. The remaining IC's are contained in TO–5 type housings and have a case tip which represents the starting or ending point for pin numbers (A through C, fig. 2–2).

### 2-4. Symbology and Terminology of Recurring Elements of Integrated Circuits

*a. NOR Gate.* The logic symbol for a NOR gate is shown in A, figure 2–3. A NOR gate is said to be enabled when one or both of the inputs (A or B) is a logic one (approximately +7.2 vdc). Enabling the NOR gate results in a logic zero (approximately 0 vdc) output (X). If all inputs are low, the gate is said to be inhibited and the output is high.

*b. Inverter.* The logic symbol for the inverter is shown in B, figure 2–3. A logic one input to an inverter results in a logic zero output. Conversely, a logic zero input results in a logic one output.

*c. Flip-Flop.* The logic symbol for a flip-flop is shown in C, figure 2–3. The flip-flop has two possible output states; Q and $\overline{Q}$ (the latter is pronounced NOT Q). Output states are controlled

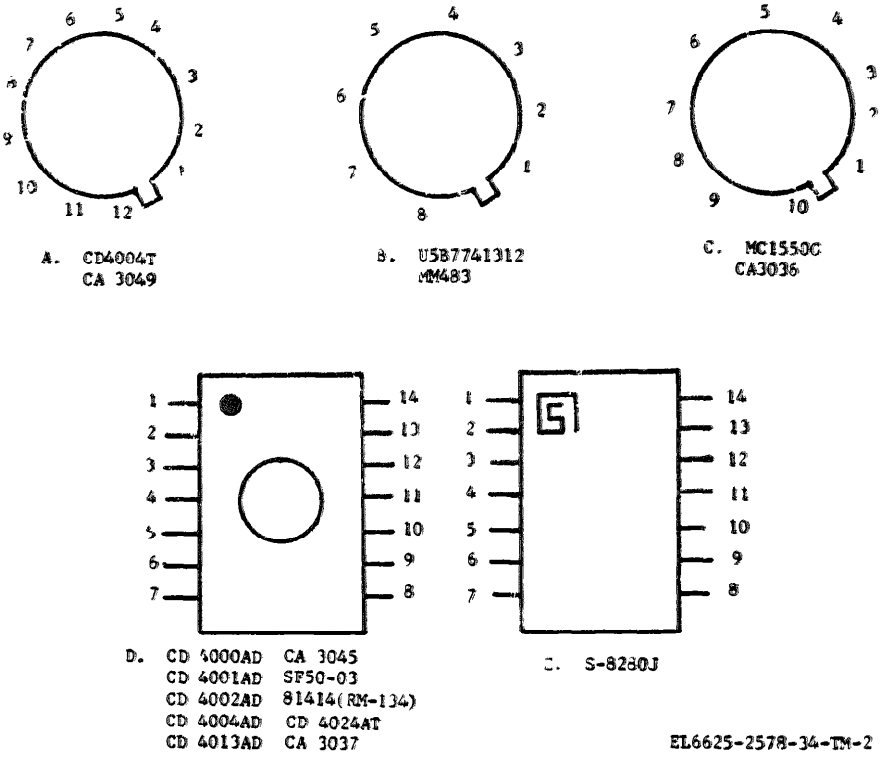



Figure 2-2. Integrated circuit pin arrangements.

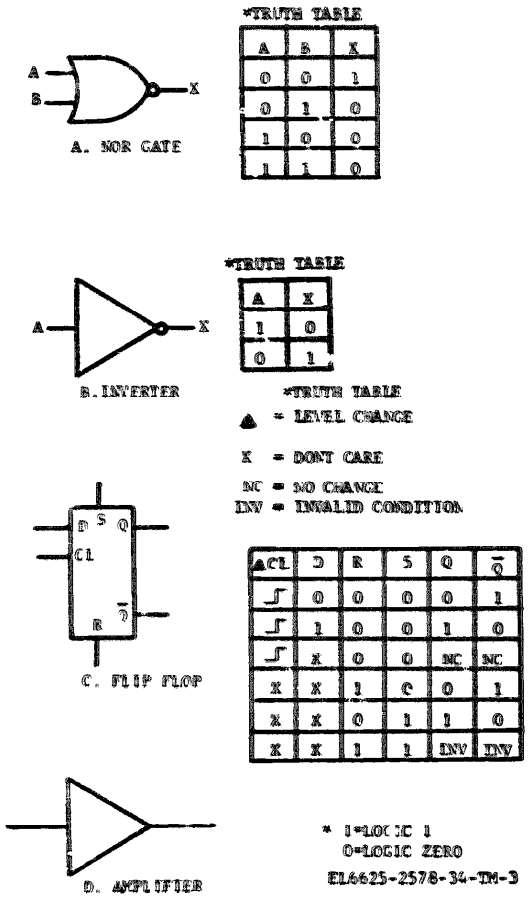



Figure 2-3. Integrated circuit logic symbols.

by the input level at the data input (in conjunction with a clock pulse) and the level at either the DC SET (if used) or DC RESET inputs. The logic level present at the data input is transferred to the Q output during the positive going transition of a clock pulse. The $\overline{Q}$ output will always be in the opposite state from the Q output. The DC SET (if used) and DC RESET inputs are independent of, and override, clock and data inputs. A logic one at the DC SET (if used) input causes the Q to become a logic one and $\overline{Q}$ a logic zero. A logic one at the DC RESET input causes Q to become a logic zero and $\overline{Q}$ a logic one. The flip-flop will remain in either state indefinitely until reversed by appropriate input signals.

*d. Amplifiers.* Amplifiers, as they are shown on schematic diagrams, are represented in D, figure 2-3. These amplifiers are operational amplifiers, although they may connect for a specific function.

## 2-5. Symbology and Terminolgy of Complete Integrated Circuits

Internal packaging and pin connection of integrated circuits is shown in figure 2-4.

*a. SF50-03.* The SF50-03 (A, fig. 2-4) is an AND input, J-K flip-flop used to divide by two. Unused inputs to the AND gates and DC SET, DC RESET, or DC PRESET are connected to +7.2 vdc. The SF50-03 is used in the 1A1A8 and 1A1A10 modules.

*b. S-8280J.* The S-2820J (B, fig. 2-4) is a decade counter connected in the BCD counting mode and is used in the 1A1A8 module. The counter has a strobed parallel-entry capability so that the counter may be preset to any desired output state. A logic one or logic zero will be transferred to the associated output when the strobe input is a logic zero. A logic zero at the reset input produces a logic zero at each output. The counting operation is performed on the falling (negative going) edge of the input clock pulse.

*c. CD-4024AT.* The CD-4024AT (C, fig. 2-4) is a seven-stage binary counter with a pulse shaper input stage. A high level at reset causes Q output of all stages to go low. The counter advances one binary count on each negative going transition at the input, pin 1.

*d. CD4000AD* The CD-4000AD (D, fig. 2-4) is a dual 3 input NOR gate, single inverter IC.

*e. CD-4001AD.* The CD-4001AD (E, fig. 2-4) is a quad 2 input NOR gate IC which is used in several modules.

*f.* CD-4013AD. The CD-4013AD (F, fig. 2-4) is a dual D flip-flop with SET/RESET IC used in several modules. The CD-4003AD is identical to the CD-4013AD except that there is no SET(s) input on a CD-4003AD. Therefore, the CD-4003AD may be used in place of the CD-4013AD if a SET input is not required.

*g. CD-4006D.* The CD-4006D (G, fig. 2-4) is an 18-stage shift register. Data is shifted through each register stage on the negative going edge of a clock pulse.

*h. Diode Matrices.* Diode matrices, part number 8141 , have some of their internal fusible-link diodes intentionally blown out. These matrices are shown on individual schematic diagrams as they actually are.

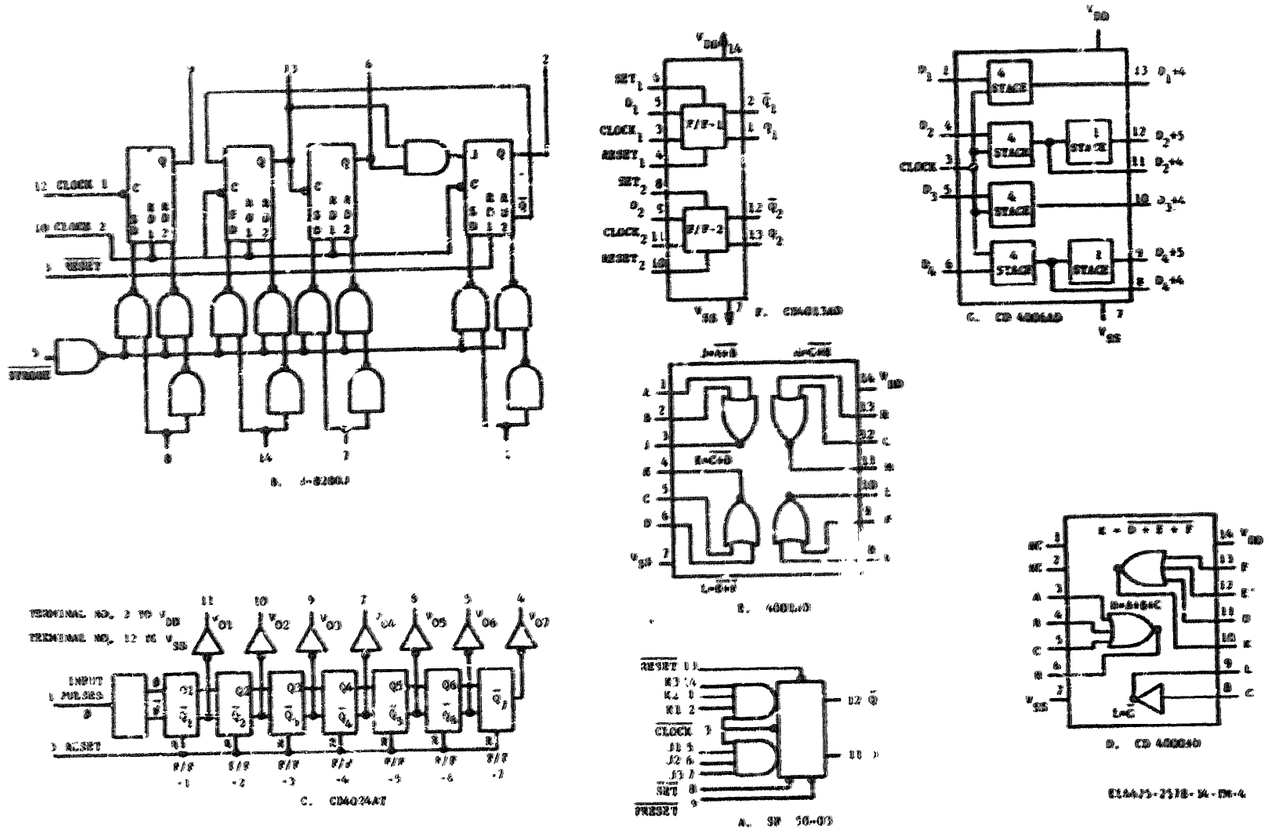


Figure 2-4. Integrated circuits logic diagram.

## Section III. GENERAL FUNCTIONING OF SECTIONS

### 2-6. General

Refer to the partial schematic or block diagrams referenced in the text and the overall block diagram (fig. 6–2), to aid in understanding the general functional description of sections and modules.

### 2-7. Program Generator

*a.* The program generator section is comprised of the following modules which are described below:

(1) Mode Control I 1A1A6

(2) Mode Control II 1A1A8

(3) Word Length Generator 1A1A9

(4) Mode Control III 1A1A11

(5) Encoder I 1A1A12

(6) Encoder Matrix 1A1A13

(7) Encoder II 1A1A14

(8) Shift Register 1A1A15

*b. Mode Control I* (fig. 2–5).

(1) Mode control I receives information from the front panel MODE switch (S7) which determines if the type of operation is to be sequential or repetitive, manual, or automatic. If the manual mode is selected, this information is decoded by the mode selection gates and applied to the sequence initiator, requiring that the START button be pressed once for every word generated. Had the automatic mode been selected, the sequence initiator would have continued to generate the necessary word start signals until the complete 64-word sequence had been achieved.

(2) The automatic mode may be interrupted or inhibited by several conditions. Power turn-on or interruption will inhibit the sequence initiator until the proper reset functions have been accomplished; pressing the START button inhibits the sequence initiator and causes the reset generator to put out a pulse (TP3) which, in turn, restarts the sequential cycle. Mode change also causes a restart resulting in initiation of the first sequential word.

(3) Mode selection information from the mode selection gates is also passed on to Mode Control III (1A1A11).

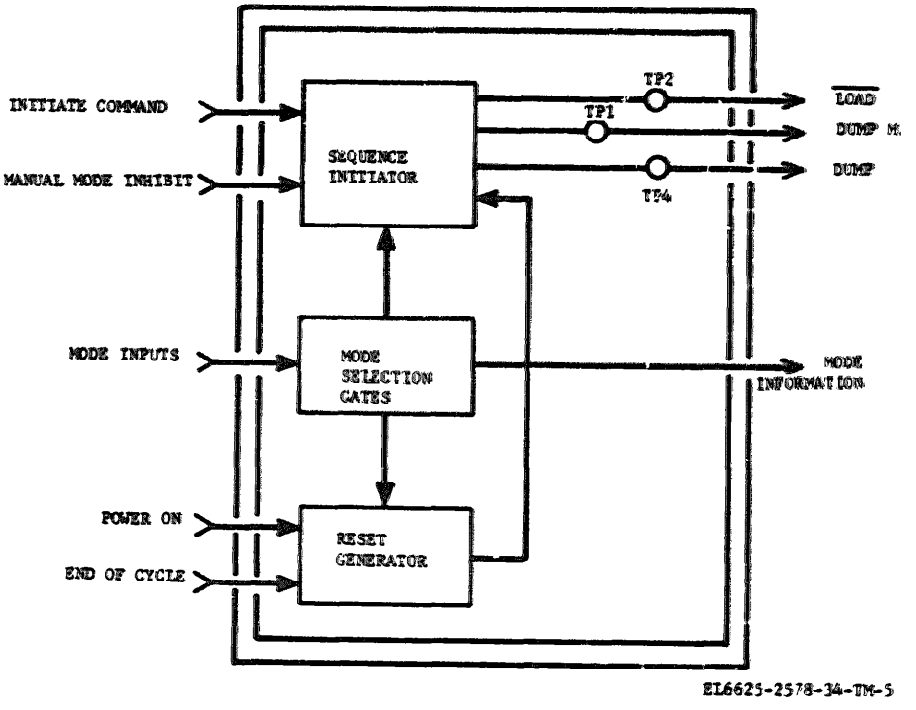



Figure 2-5. Mode control I, simplified block diagram.

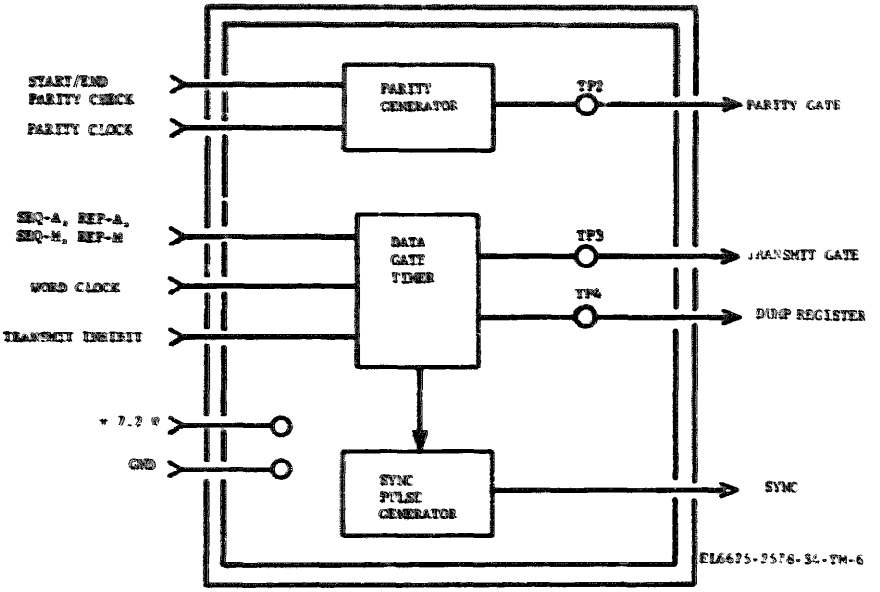



Figure 2-6. Mode control II, simplified block diagram.

*c. Mode Control II* (fig. 2–6).

(1) The Mode Control II module performs two basic functions, parity bit control and recycle time regulation. The parity generator receives start and end parity check commands from the Word Length Generator (1A1A9). The commands and a parity clock from the Shift Register (1A1A15) produce a parity gate (TP2). This parity gate will insert the proper bit in the message to assure correct parity.

(2) The delay between successive messages must be controlled in order to prevent command overlap, eliminate the effects of any possible switch bounce, and to provide enough time for proper message reception by the AN/USQ–46 or AN/USQ–46A. The data gate timer determines this delay by combining mode information from the front panel with a word clock pulse. If a transmit inhibit signal is not present, a dump register (TP4) and a transmit gate (TP3) signal, in the correct time sequence to begin a message, is provided as outputs. In the manual mode, the word is transmitted as soon as the START button is pressed and a 0.5-second delay time follows the end of the message. A new message cannot begin until this delay has elapsed. In the automatic mode, a 1-second delay time commences when the START button is pressed, and after this delay, the word is transmitted. At the end of the word, another 1-second delay is instituted before the transmission of the next word. The delayed reset pulse may be seen at TP1.

(3) An auxiliary function of the Mode Control II module is the development of the sync pulse to the front panel SYNC Connector, 1A1-A18J4.

*d. Word Length Generator* (fig. 2–7).

(1) The Word Length Generator has four basic functions, one of which is to generate a pulse when power is turned on. The reset generator provides a POWER ON RESET pulse of approximately 50 msec in duration and outputs this signal to the Encoder II module (1A1A14), the Mode Control I module (1A1A6) and Mode Control III module (1A1A11).

(2) When the START button on the front panel is pressed, the synchronizer gates this information along with the clock input in order to produce an activate synchronizer pulse which is synchronous with all internally generated clocks.

(3) Should a type 3 message be desired, the message type decoder will determine this from the front panel switch positions and send this information to the audio gate generator. The 0.5-second delay which would normally follow the end of a manual word is inhibited to permit a 20.5-second audio gate to be delivered to the VCXO (1A1A1).

(4) The word length detector will detect the start parity check and end parity check points by performing a count of its gated clock inputs (TP1) and will also output an end word signal (TP2) when the 18 or 24 message bits

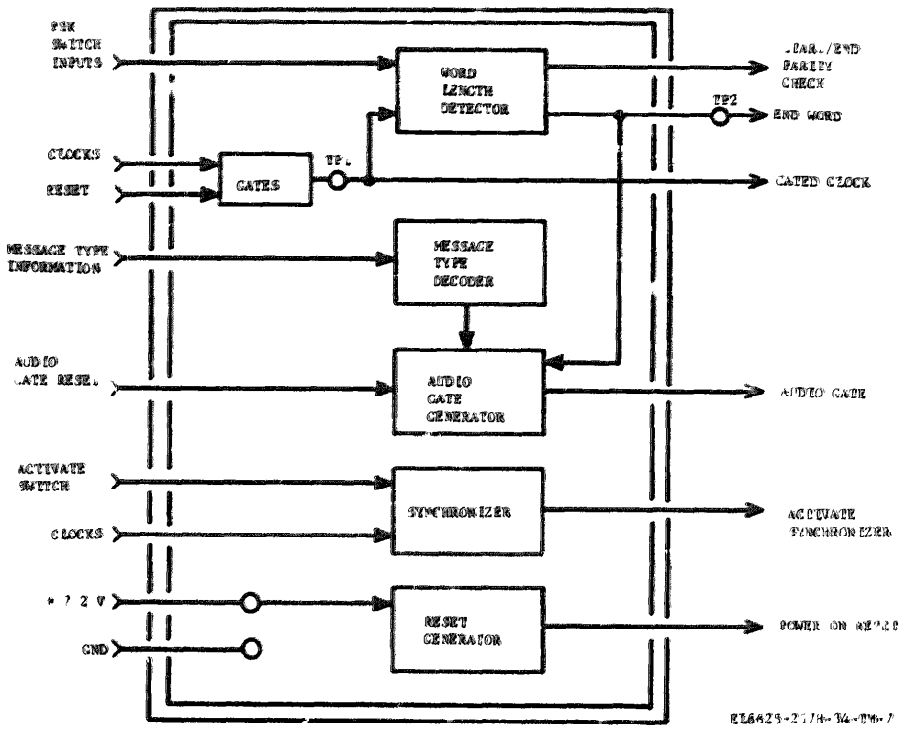



Figure 2-7. Word length generator, simplified block diagram.

have been completed (determined by message type).

*e. Mode Control III* (fig. 2–8).

(1) An input clock from the Encoder II module (1A1A14) is received by the clock divider circuit which then divides the clocks into two frequencies; slow (75 Hz), and fast (300 Hz). These clocks are utilized by modules 1A1A6, 1A1A8, 1A1A9, and 1A1A12.

(2) The burst generator gate signal from Encoder II module (1A1A14) is delayed by the burst generator gate delay circuit in order to prevent a premature command initiation. This signal goes to the Mode Control I module (1A1A6).

(3) Information from the front panel mode switches is used by the mode decode matrix along with FSK switch information, to determine the proper time sequence for the VCXO GATE (TP1) and the 1 kHz GATE (TP5). The control gates also determine the modulation frequency applied to the VCXO (1A1A1) by selecting VCXO B or VCXO C (TP2).

*f. Encoder I* (fig. 2–9).

(1) The function of the Encoder I module is to produce an output which is used as the units input to the Encoding Matrix (1A1A13) which in turn will determine what word is to be generated.

(2) Information from the front panel mode switches is utilized by a shift register to determine if a count inhibit signal should be present. If in the repetitive mode, the shift register will be inhibited and the front panel program switch information will be routed through the sequential/manual gates to the Encoding Matrix (1A1A13).

(3) Should a sequential mode have been selected, the shift register will be advanced with each end word input until a count carry (TP1) is generated to the Encoder II module (1A1A14). This count sequence continues until all 64 words have been transmitted. Then the signal $\overline{9\text{–}2}$ and information from the Encoder II module (1A1A14) will prevent the sequential coding advancement. When in a sequential mode the program switch information to the sequential/manual gates is inhibited and shift register information is sent to the Encoding Matrix (1A1A13).

*g. Encoder Matrix* (fig. 2–10). The Encoding Matrix, containing two diode matrices, senses and encodes the states of the two encoder regis-

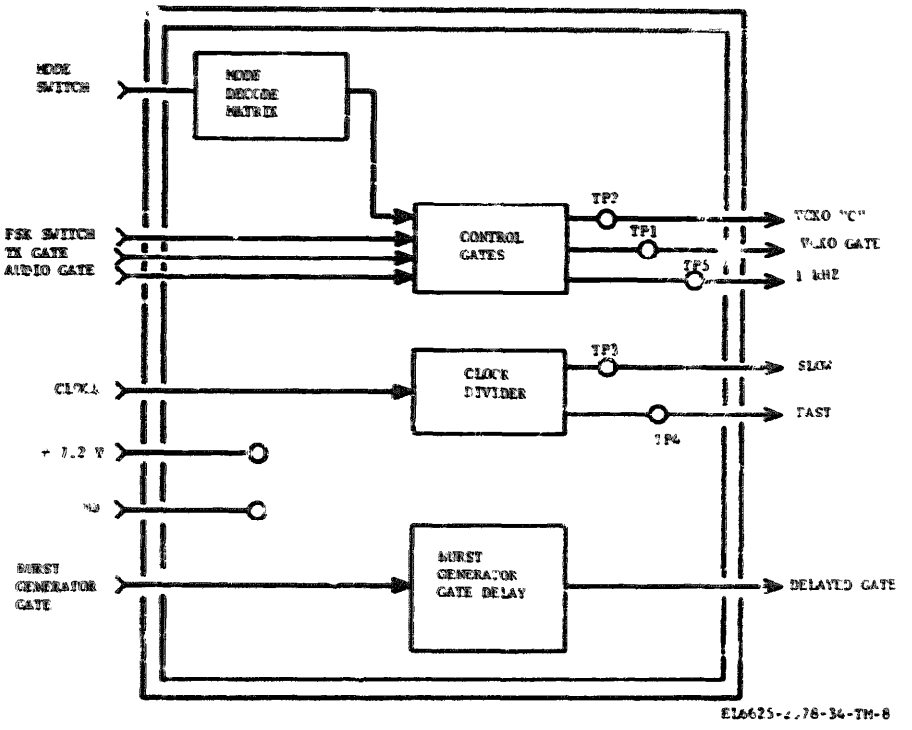



Figure 2-8. Mode control III, simplified block diagram.

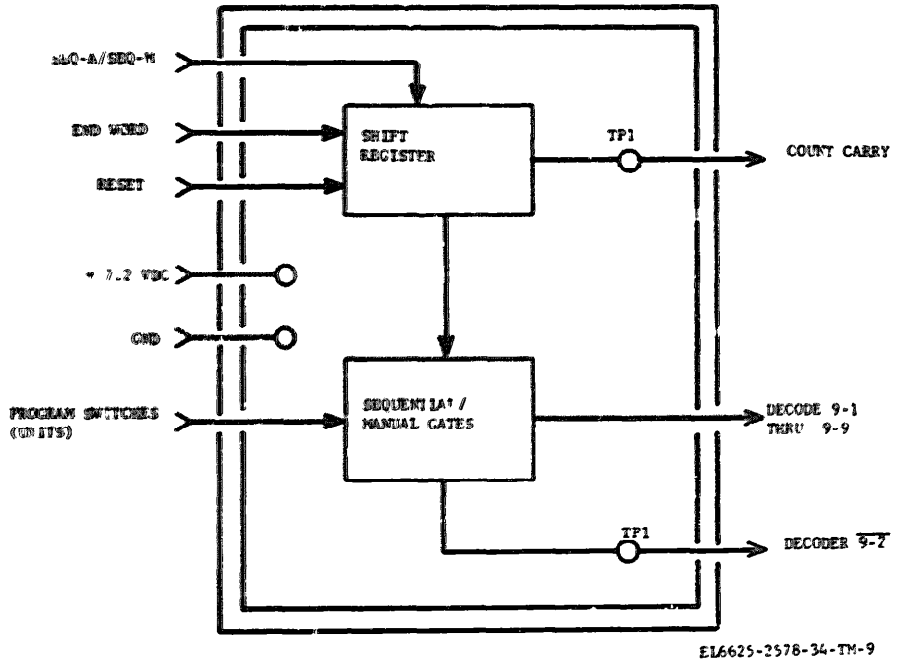



Figure 2-9. Encoder I, simplified block diagram.

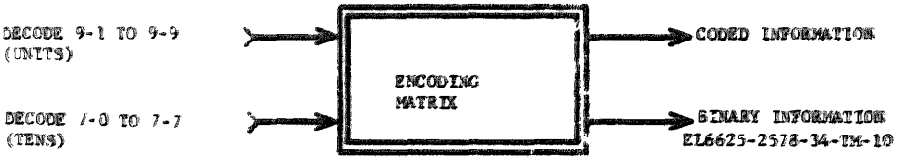



Figure 2-10. Encoder matrix, simplified block diagram.

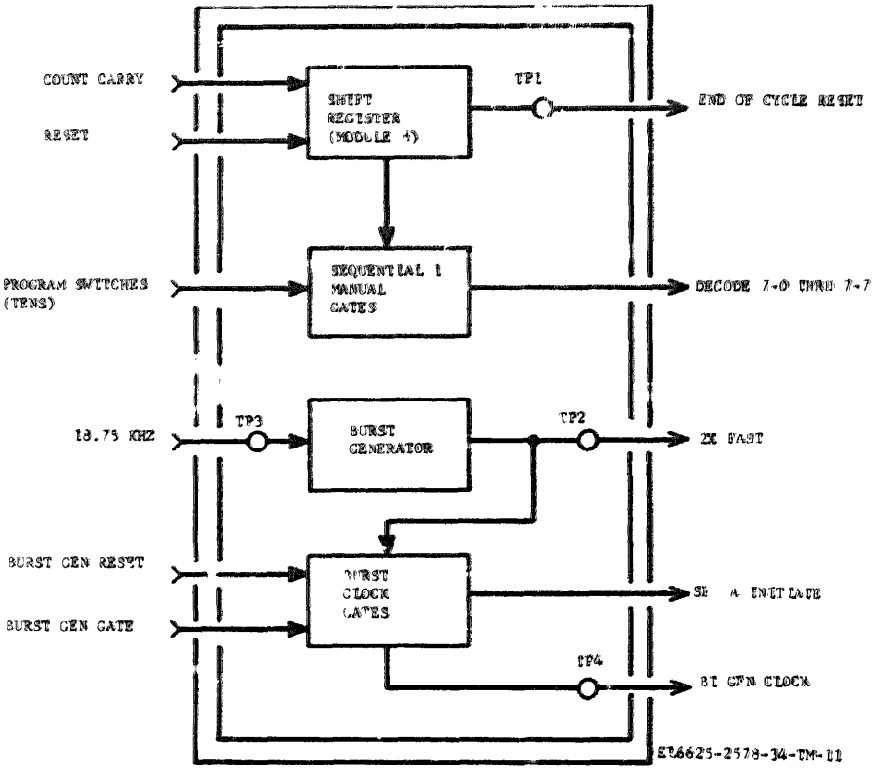



Figure 2-11. Encoder II, simplified block diagram.

ters. Encoder I (1A1A12) and Encoder II (1A1A14). One matrix decodes and outputs 6-bit binary information while the other matrix decodes and outputs 6 bit coded information. The code and binary signals are routed to the Shift Register (1A1A15) where they are used to form the transmitted word.

*h. Encoder II* (fig. 2–11).

(1) Encoder II functions in a manner very similar to that of Encoder I (1A1A12). Encoder I supplies a count carry input to Encoder II while both use the common reset signal. When the complete word sequence has been executed, an end of cycle reset is generated (TP1).

(2) Information from the shift register is gated with the program switches inputs (tens) to provide an output to the Encoding Matrix (1A1A13)

(3) An 18.75 kHz signal (TP3) from the Reference Generator (1A1A10) in the Frequency Synthesizer section, is injected into the burst generator which divides this input down to the 2X Fast frequency (600 Hz, TP2). This signal is then controlled by the burst clock gates to produce a gated clock (TP4) to the Shift Register (1A1A15) and a timed SEQ A INITIATE pulse to Mode Control I module (1A1A6,.

*i. Shift Register* (fig. 2–12). The Shift Register receives 6-bit binary data from the Encoding Matrix (1A1A13). When a LOAD DELAYED

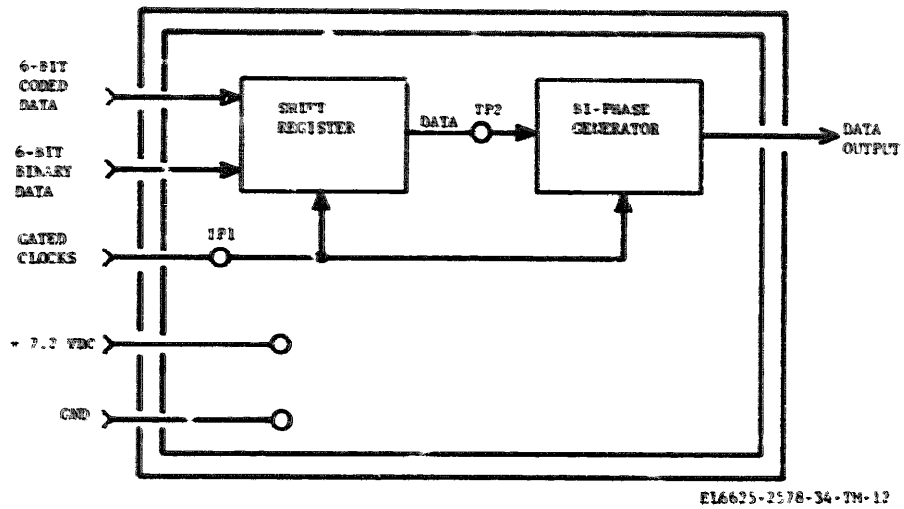



Figure 2-12. Shift register, simplified block diagram.

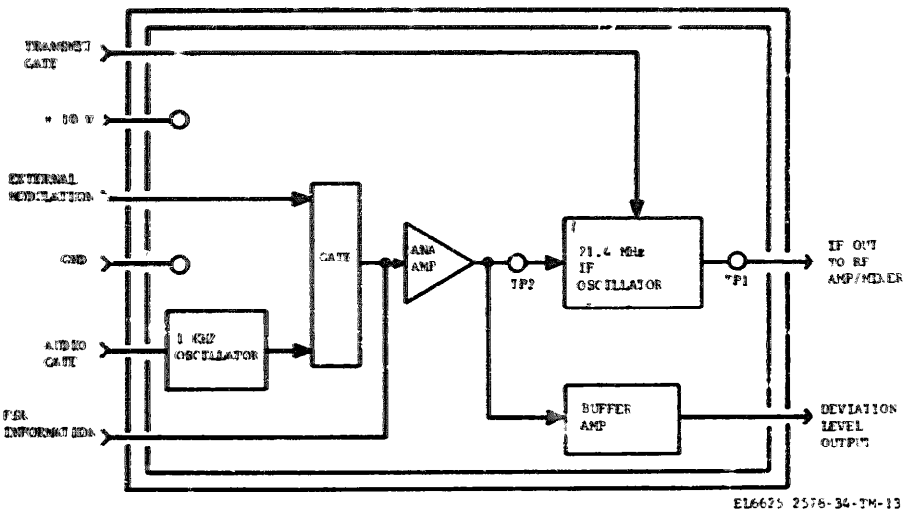



Figure 2-13. VCXO, simplified block diagram.

**command is received, this information is loaded into the shift register cells while the first 9 cells are reset by the LOAD DELAY command. When gated clocks are generated (TP1), the information in the shift register is shifted out (TP2) to the biphase generator. The biphase generator converts the input data into Manchester coded data which is applied to the Mode Control III module (1A1A11).**

2-8. Modulation Steering and Control Section.

***a.*** **This section is comprised of the Voltage Controlled Crystal Oscillator (VCXO) 1A1A1 (fig. 2–13).**

***b.*** **The VCXO is the source of the 21.4 MHz carrier frequency (IF). The front panel mode switch has three positions which will affect the modulation of the VCXO and are indicated by the abbreviations CAL (calibrate), INT (internal), and EXT (external). When the MODE switch is in INT a 1 kHz oscillator is enabled which produces the modulation signal during the 1 kHz GATE pulse time. It is possible to provide modulation from an external source by injecting a signal into the front panel EXT MOD IN connector 1A1A18J2 while the MODE switch is in the EXT position The third switch position (CAL) provides no modulating signal to the IF**

oscillator. Therefore, an unmodulated 21.4 MHz signal will be seen at TP1. The internal or external modulations signals are gated with FSK information to the analog amplifier. The output of the analog amplifier at TP2 is the modulation signal to be used by the IF oscillator. Presence of the VCXO GATE is required to turn on the IF oscillator.

## 2-9. Frequency Synthesizer Section

*a.* This section is comprised of the following modules which are described below:

(1) Temperature Compensated Crystal Oscillator (TCXO) 1A1A16

(2) Reference Generator 1A1A10

(3) Synthesizer Mixer 1A1A4

(4) Programmable Divider 1A1A5

(5) Loop Filter/VCO 1A1A3

*b.* The Temperature Compensated Crystal Oscillator generates an output of 3.75 MHz with ±1 ppm stability over its entire input voltage range of 10–16 vdc. The 3.75 MHz signal may be monitored at TP2 of the Reference Generator module (1A1A10).

*c. Reference Generator* (fig. 2–14).

(1) The Reference Generator receives a 3.75 MHz input from the TCXO (1A1A6) and produces three outputs. The 3.75 MHz input is fed to a bandpass filter which selects the fourth harmonic of 3.75 MHz, or 15 MHz at its output. This 15-MHz signal then goes through a times six multiplier stage to produce 90 MHz at its output (TP1). This 90 MHz is applied to the Synthesizer/Mixer module (1A1A4).

(2) The 3.75 MHz input (TP2) also goes to a divide-by-two-circuit whose output of 1.875 MHz (TP3) is then used by two circuits. One of these circuits is a divide-by-100 device which will produce a final output of 18.75 kHz to be used by the Programable Divider module (1A1A5).

(3) The spectrum generator also receives the 1.875-MHz square wave input and transforms this into a spectrum output to the Synthesizer/Mixer module (1A1A4). The filters in the Synthesizer/Mixer will utilize the 25th to 33rd harmonics of the spectrum output (TP4).

*d. Synthesizer Mixer* (fig. 2–15).

(1) The Synthesizer/Mixer mixes input frequencies from the Reference Generator (1A1A10) with the LO frequency from the Loop Filter/VCO (1A1A3) and, in conjunction with a tuning voltage from the RF CHANNEL NUMBER switches, produces an output clock frequency for use by the Programable Divider (1A1A5).

(2) The first mixer mixes 90 MHz from the Reference Generator with the LO frequency

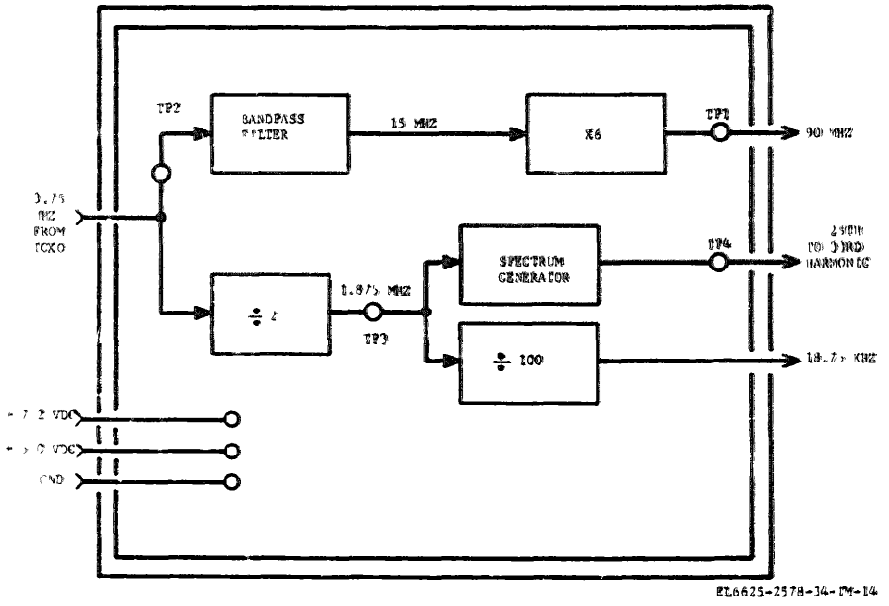



Figure 2-14. Reference generator, simplified block diagram.

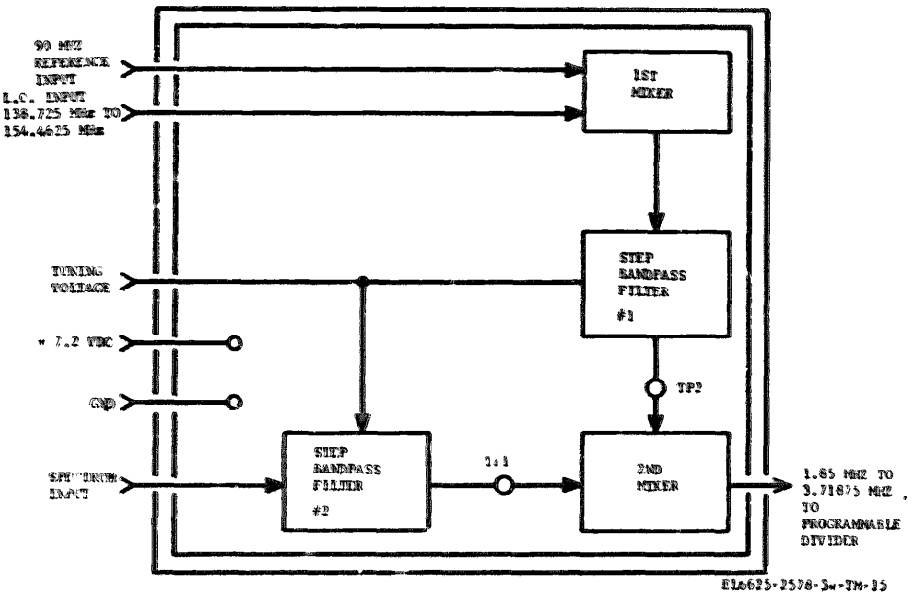



Figure 2-15. Synthesizer mixer, simplified block diagram.

(138.725 to 154.4625 MHz) to produce a difference frequency (48.725 to 64.4625 MHz) at its output. This output goes to the step bandpass filter one which uses the tuning voltage input to select the proper output frequency.

(3) Step bandpass filter two uses the spectrum output (25th to 33rd harmonic) from the Reference Generator, along with tuning voltage to select an output frequency (46.875 to 61.875 MHz).

(4) The outputs from bandpass filter one and bandpass filter two are mixed by the second mixer to produce an output which may range from 1,85 to 3.71875 MHz according to the RF channel number selected. The outputs of bandpass filters one and two may be monitored at test points TP2 and TP1 respectively.

*e. Programable Divider* (fig. 2–16).

(1) The Programable Divider module receives the analog signal output from the Synthesizer/Mixer (1A1A4) second mixer and passes it through a pulse shaper. This enables the signal at TP1 to have a clocking edge transition time adequate to properly clock the programable divider. Information fron the front panel RF CHANNEL SELECT switches is decoded by the diode matrices and is then used to preset the programable divider so that any count between 296 and 595 may be obtained. The strobe pulse (TP2) from the programable divider is used by the Loop Filter/VCO module (1A1A3).

(2) The 18.75 kHz from the Reference Generator (1A1A10) is divided by three and the resultant 6.25 kHz signal is routed to the Loop Filter/VCO.

*f. Loop Filter/VCO* (fig. 2–17).

(1) The strobe pulse and 6.25-kHz reference frequency inputs to the Loop Filter/VCO permit the frequency discriminator, phase detector and loop filter to generate an error voltage to the VCO. The output from the VCO (LO frequency) is then used to modify the frequency synthesizer circuits in such a manner as to become self-correcting for frequency stability.

(2) A strobe pulse from the Programable Divider (1A1A5) is injected into the frequency discriminator which provides a course adjustment. The coarse adjust output pulse, if other than a symmetrical square wave, signifies that the VCO is not at the frequency of the selected RF CHANNEL NUMBER. A loop filter converts the coarse adjust output signal from the frequency discriminator into a dc error voltage to the VCO. If the VCO is tuned below the proper frequency, the dc error voltage is raised in value. Similarly, if the VCO is tuned above the proper

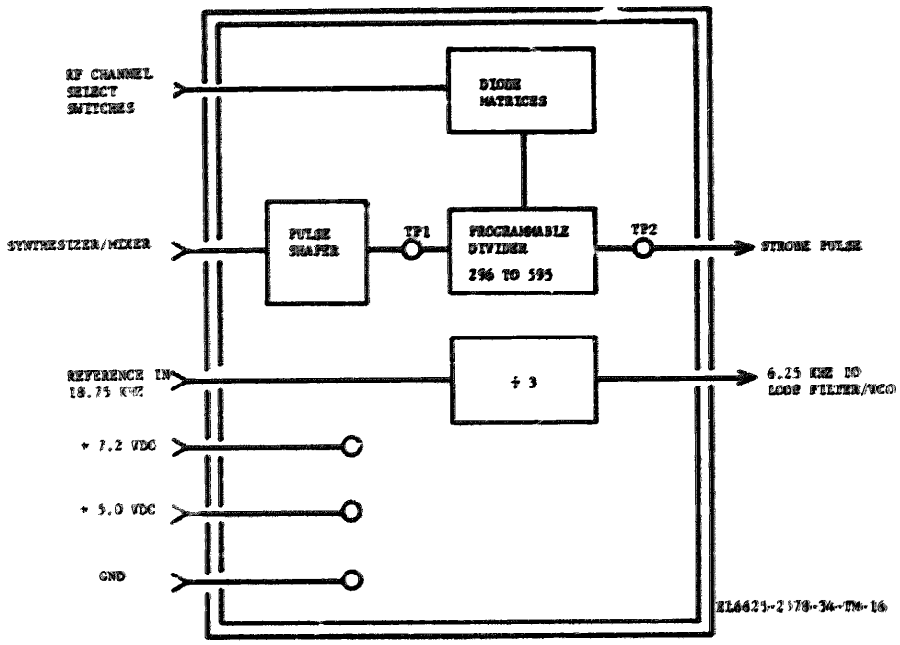



Figure 2-16. Programmable divider, simplified block diagram.

frequency, the dc error voltage is lowered in value. At the proper frequency, a constant dc error voltage is maintained.

(3) To assure greater accuracy, the strobe pulse also connects to a phase detector. The 6.25-kHz signal (TP1) from the divide-by-three circuit is phase-compared to the strobe pulse (TP2). Differences in phase between the two input signals cause a fine adjust signal to be added to the coarse adjust signal at the loop filter. Slight changes will then be made to the value of the dc error voltage (TP4).

(4) The VCO produces the tunable RF output signal (LO frequency). The error voltage (TP5) in conjunction with a tuning voltage input permits an approximate range of 130 to 154 MHz using nine discrete bands which accommodate 300 channels each. Buffer amplifiers isolate the VCO from the RF Mixer/Amplifier (1A1A7) (TP6) and the Synthesizer/Mixer (1A1A4).

## 2-10. RF Amplifier/Detector Output Section

This section is comprised of the RF Mixer/Amplifier (1A1A7) and Detector Output (1A1A2) modules.

*a. RF Amplifier/Mixer* (fig. 2–18).

(1) The RF Mixer/Amplifier receives the local oscillator frequency (138.725 to 154.4625 MHz) from the Loop Filter/VCO module (1A1-A3) and applies it to an attenuator pad which reduces signal amplitude to an operable limit and provides a 50-ohm impedance termination. The signal then passes on to gain control attenuator, which is an amplifier with manual gain adjust provisions, and then on to the balanced mixer. The IF frequency (21.4 MHz) from the VCXO module (1A1A1) is reduced in amplitude by a 10-db pad and becomes the second input to the balanced mixer. The combined frequencies are now the output from the balanced mixer and this output is passed through two series RF amplifiers which serve as the RF level adjustment in combination with the front panel LEVEL SET control.

(2) In order to permit proper tracking throughout the nine available tuning steps variable capacitors C15, C24, C32, and C41 are provided. The final RF OUT to the RF Detector-Output module (1A1A2) may be monitored at TP1.

*b. Detector Output* (fig. 2–19).

(1) The front panel meter is capable of displaying RF LEVEL and DEVIATION LEVEL by utilizing output signals from the Detector-Output module. The DEVIATION LEVEL sig-

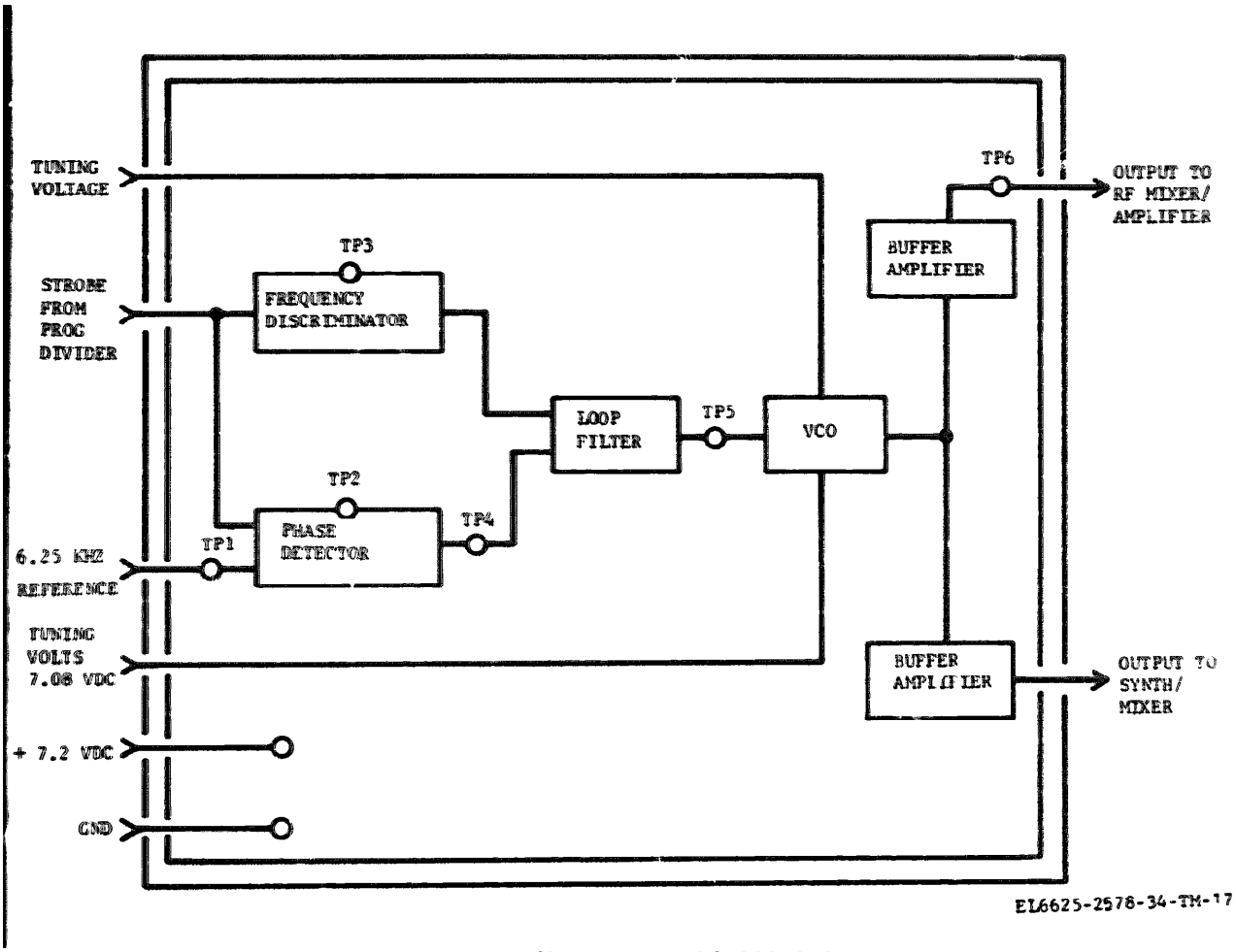



Figure 2-17. Loop filter/VCO, simplified block diagram.

nal from the VCXO (1A1A1) may be checked at TP3, before the signal enters the deviation detector. The two detected outputs may be monitored at TP4 and TP5, which are test points for external meter attachment. Resistor R7 provides meter zero adjustment while R14 is the deviation calibrate adjustment.

(2) There are two inputs to the detector output: tuning voltage from the RF CHANNEL NUMBER switches and an RF signal output from the RF Mixer/Amplifier (1A1A7). The RF signal is processed through an RF amplifier, using C6 and C16 as adjustments, and the output is fed to both attenuator pads and an RF detector. After the signal passes through the fixed attenuator pads it is applied to the front panel step attenuators. The RF detector performs the same basic function as did the deviation detector; the RF detector provides an output level to the front panel meter for calibration purposes. Resistor R19 serves as the meter zero adjustment while R29 is the calibration adjustment. An external meter may be connected to test points TP1 and TP2 for test purposes.

## 2-11. Power Supply/Regulator Section 1A1A17 (fig. 2-20)

The operating voltages for the Radio Test Set originate in the Power Supply/Regulator. Source voltage is +12 vdc regulated which is provided by the Power Supply PP-6446A/USQ-46. Each regulated output voltage passes through an associated series regulator. The +7.2 and +3.6 vdc regulated operating voltages have additional stability due to the inclusion of a constant current source (No. 1) between the source voltage and the common series regulator. Constant current source No. 2 performs the same function for the +5 vdc regulated operating voltage. If desired, a battery may be used in place of the power supply as long as its output exceeds 11.5 volts under load.

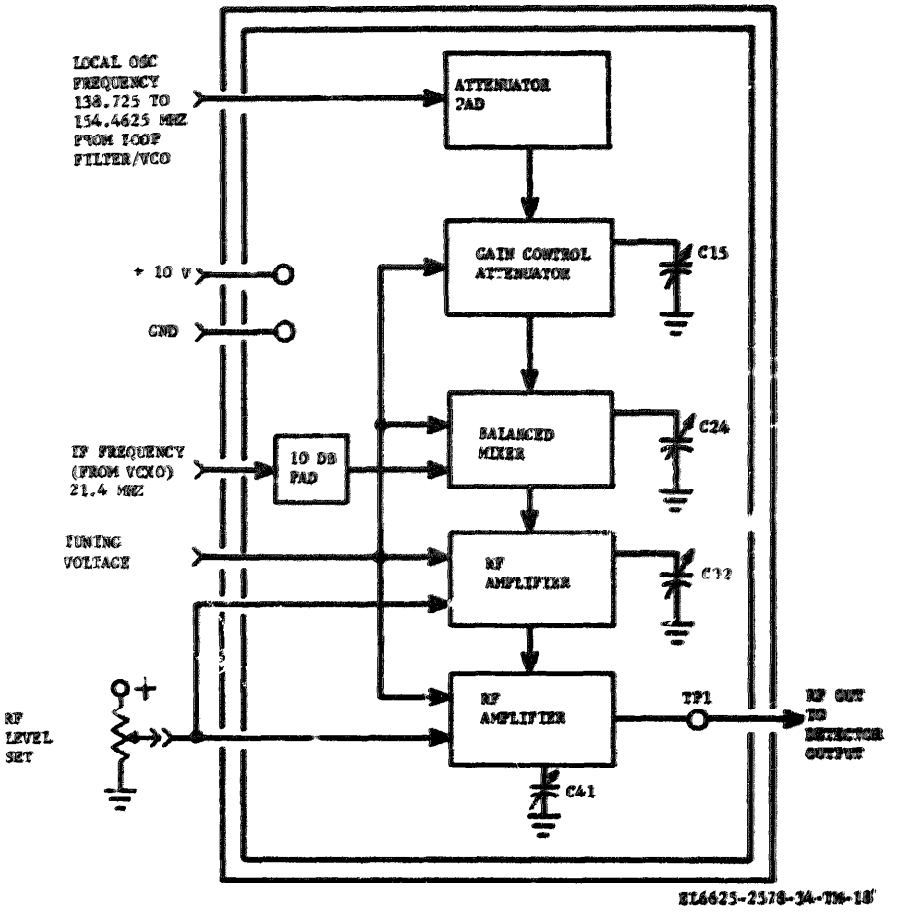



Figure 2-18. RF mixer/amplifier, simplified block diagram.

2-12. Front Panel Assembly 1A1A18.

The front panel assembly contains all the switches, potentiometers, meters and connectors necessary to properly utilize the radio test set. Following is a listing of the various controls and switches and the modules to which they connect.

*a.* Attenuator switches (Detector-Output Module 1A1A2).

*b.* RF CHANNEL NUMBER switches (Synthesizer/Mixer 1A1A4, RF Amplifier/Mixer 1A1A7, Loop Filter/VCO 1A1A3, Programable Divider 1A1A5).

*c.* MODE switch (Mode Control I 1A1A6, Mode Control III 1A1A11).

*d.* MESSAGE switch (Word Length Generator 1A1A9).

*e.* FSK switch (VCXO 1A1A1).

*f.* PROGRAM switches (Encoder I 1A1A12, Encoder II 1A1A14).

*g.* METER switch (Front Panel Assembly 1A-1A18, Detector/Output 1A1A2).

*h.* RF LEVEL SET potentiometer (RF Amplifier/Mixer 1A1A7).

*i.* DEVIATION SET Potentiometer (VCXO 1A1A1).

*j.* Meter (Front Panel Assembly 1A1A18).

*k.* START button (Word Length Generator 1A1A9).

*l.* Fuse (power supply).

*m.* SYNC output jack (Mode Control II 1A1-A8).

*n.* VIDEO output jack (Shift Register 1A1-A15).

**o. RF output jack (Front Panel Assembly 1A1-A18).**

**p. EXTERNAL MODULATION input jack (VCXO 1A1A1).**

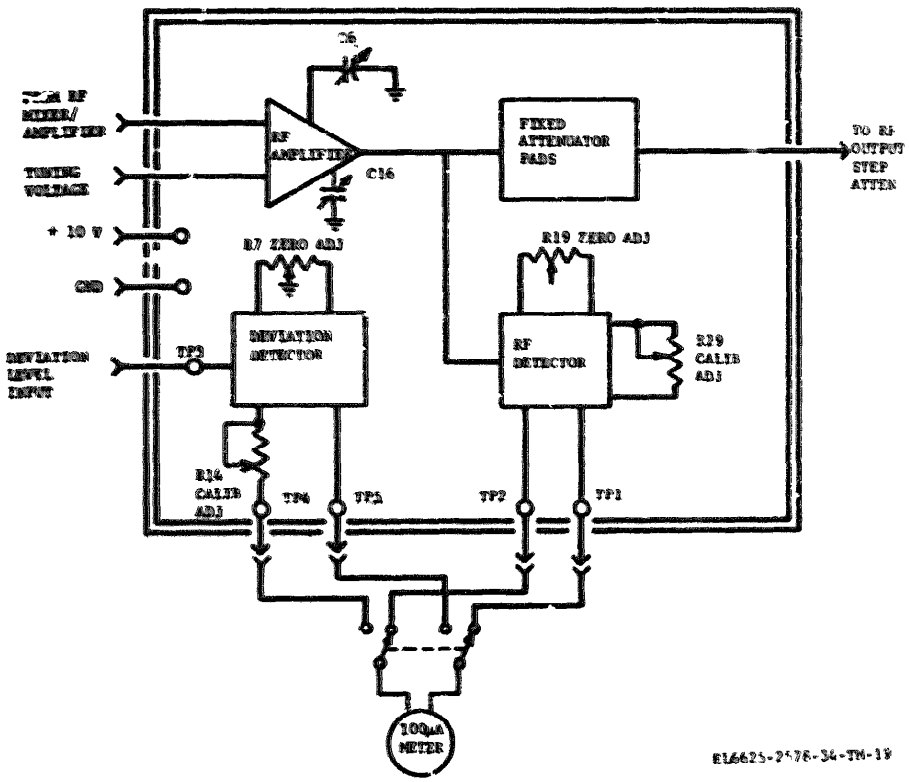



Figure 2-19. Detector output, simplified block diagram.

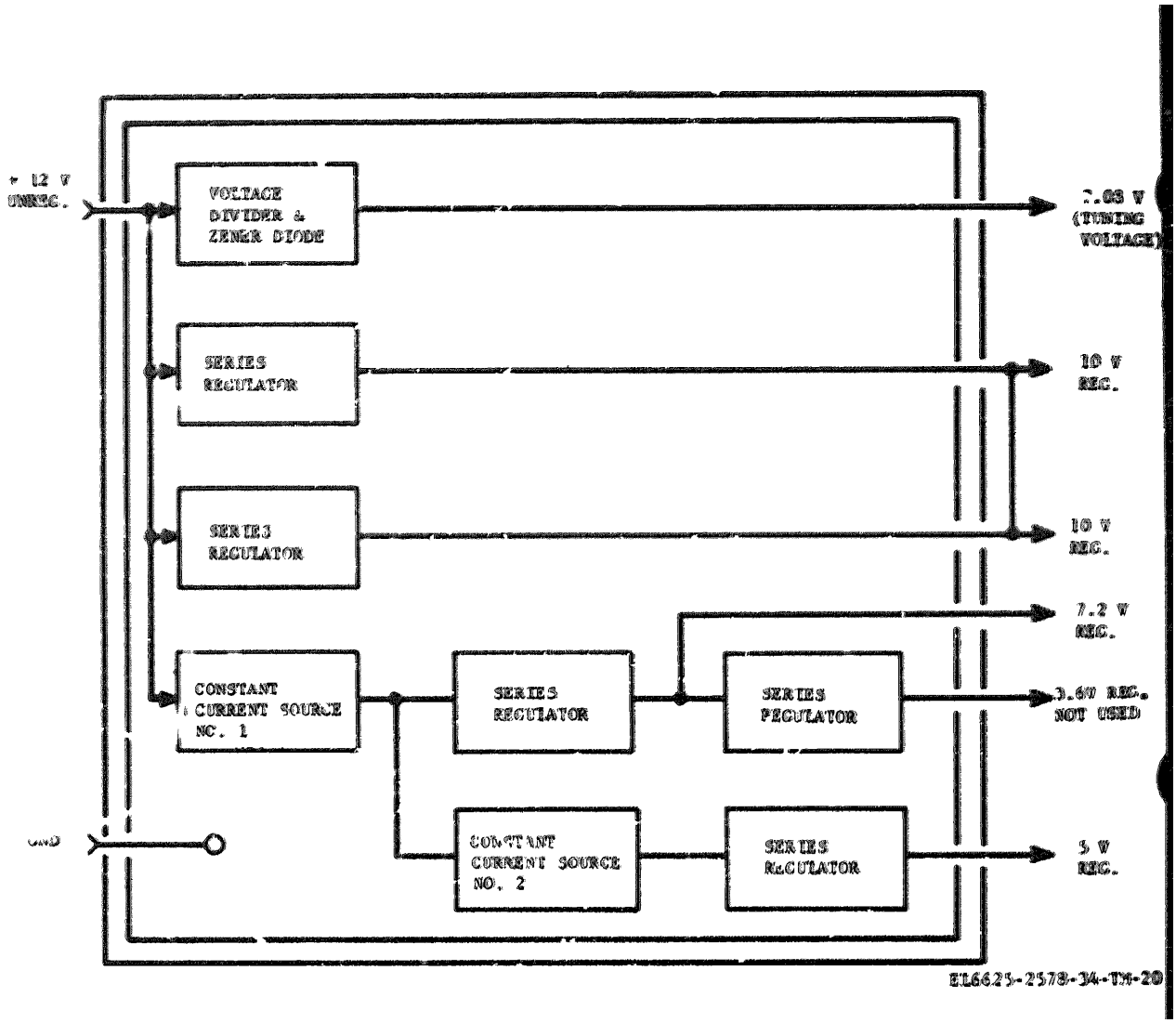



Figure 2-20. Power supply/regulator, simplified block diagram.

## Section IV. DETAILED FUNCTIONING OF TEST SET MODULES

### 2-13. General.

To aid in understanding detailed functioning of the Radio Test Set, the basic structure of an output data word is described in paragraphs 2–14 through 2–16.

### 2-14. Radio Test Set Data Word Structure

a. A complete Radio Test Set data word may contain 10 or 16 (short or long word) word bits plus an eight-bit PREAMBLE, as shown in A, figure 2–21. The PREAMBLE bits must always be logic zeros. The first word bit (SYNC bit) must always be a logic one. The two message type bits (2 and 3) may be any possible combination, depending on the type of message to be initiated (refer to paragraph 2–15 for a definition of the four message types). Address (ID) bits 4 through 9 may be logic ones or zeros depending upon which one of the possible 64 addresses are being initiated. (Refer to paragraph 2–16 for the logic one or zero bit levels for each of the 64 addresses.) Bit 10 is the parity bit, which will be a logic one or zero depending on how many logic one bits are in the six address bits. Bit 10 will be a logic one if there are an even number of ones in address bits or a logic zero if there are already an odd number of ones. The six message bits (11 through 16) are added when a long word is to be generated. These bits may be any combination of logic ones or zeros.

*b.* Although a data word is formed in binary, the actual output consists of biphase data bits as shown in B, figure 2–21.

## 2-15. Message Types

*a.* The Radio Test Set is capable of generating four message types; 1, 2, 3 and 4. Message types 1 and 4 correspond to short data words and types 2 and 3 correspond to long data words. Short words consist of 10 data bits plus 8 preamble bits and long words consist of 16 data bits plus 8 preamble bits. Table 2–1 lists the message types and the appropriate bit levels required for each type message. Although the four message types can be selected, an RF monitor can only react to the ID and parity bits. The six message bits (11 through 16) are routed through the RF monitor logic circuits to an external display connector on the front panel.

Table 2-1. Message Type Identification.

| Message type | Bit condition 2 and 3 | |
|---|---|---|
| 1 | 0 | 0 |
| 2 | 0 | 1 |
| 3 | 1 | 0 |
| 4 | 1 | 1 |

*b.* A type 2 message contains six message data bits which simulates data stored in a remote sensor event counter. The six message data bits (11 through 16) identify the total number of accumulated events that may have been detected by a sensor (events 0 through 63). Table 2–2 shows the method of event coding.

Table 2-2. Message Type 2 Coding.

| Number of events | Bit number 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 63 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 1 | 2 | 4 | 8 | 16 | 32 |

*c.* When a message type 3 is selected, the six message data bits indicate the current sensor operating mode and sensitivity setting. This data is coded as shown in table 2–3. The sensitivity settings are common to both sensor operating modes.

Table 2-3. Mesage Type 3 Coding.

| Sensor mode | | | Bit number | | | | Gain setting |
|---|---|---|---|---|---|---|---|
| BITS | 11 | 12 | 13 | 14 | 15 | 16 | |
| | | | 1 | 0 | 0 | 1 | 1 |
| RT | 0 | 1 | 1 | 0 | 1 | 0 | 2 |
| | | | 0 | 0 | 1 | 1 | 3 |
| NRT | 1 | 0 | 1 | 1 | 0 | 0 | 4 |
| | | | 0 | 1 | 0 | 1 | 5 |
| | | | 0 | 1 | 1 | 0 | 6 |

## 2-16. Address codes

Table 2–4 lists the full complement of 64 addresses with their corresponding bit level.

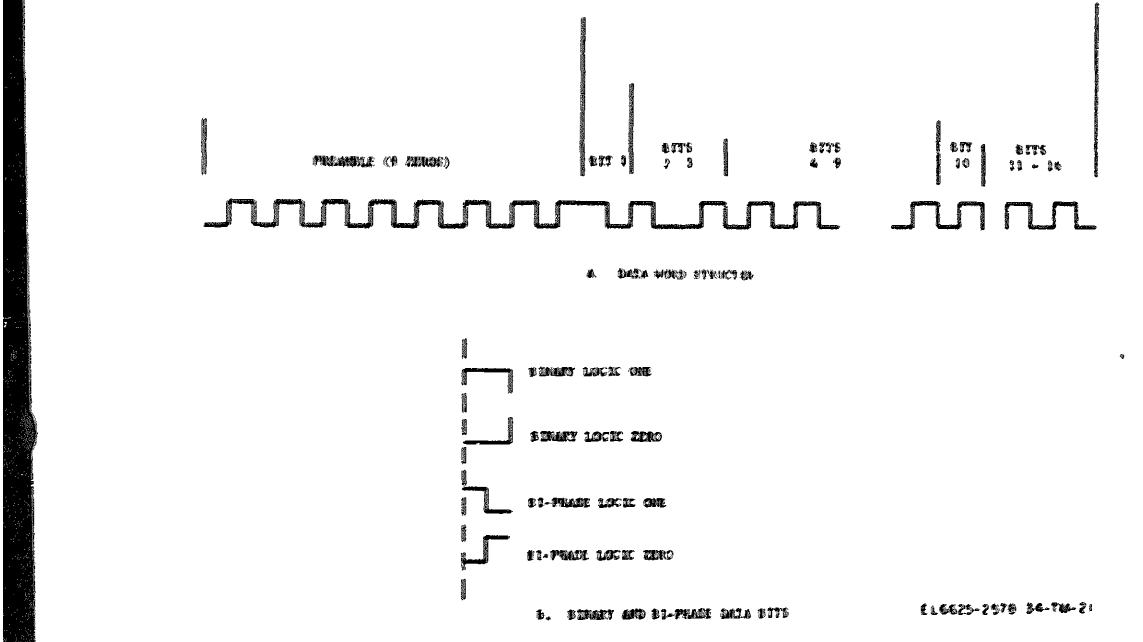



Figure 2-21. Typical radio set data word.

Table 2-4. Radio Test Set Address Codes

| Address | Bits 4 | 5 | 6 | 7 | 8 | 9 | Address | Bits 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 36 | 0 | 0 | 1 | 0 | 1 | 1 |
| 2 | 0 | 1 | 0 | 1 | 1 | 0 | 37 | 0 | 0 | 1 | 1 | 0 | 1 |
| 3 | 0 | 1 | 0 | 1 | 1 | 1 | 38 | 0 | 0 | 1 | 1 | 1 | 0 |
| 4 | 0 | 1 | 1 | 0 | 0 | 1 | 39 | 0 | 0 | 1 | 1 | 1 | 1 |
| 5 | 0 | 1 | 1 | 0 | 1 | 0 | 41 | 0 | 1 | 0 | 0 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 | 1 | 1 | 42 | 0 | 1 | 0 | 0 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 | 0 | 1 | 43 | | 1 | 0 | 0 | 1 | 1 |
| 8 | 0 | 1 | 1 | 1 | 1 | 0 | 44 | 1 | 0 | 0 | 0 | 0 | 1 |
| 9 | 0 | 1 | 1 | 1 | 1 | 1 | 45 | 1 | 0 | 0 | 0 | 1 | 0 |
| 11 | 1 | 0 | 0 | 1 | 0 | 1 | 46 | 1 | 0 | 0 | 0 | 1 | 1 |
| 12 | 1 | 0 | 0 | 1 | 1 | 0 | 47 | 1 | 1 | 0 | 0 | 0 | 1 |
| 13 | 1 | 0 | 0 | 1 | 1 | 1 | 48 | 1 | 1 | 0 | 0 | 1 | 0 |
| 14 | 1 | 0 | 1 | 0 | 0 | 1 | 49 | 1 | 1 | 0 | 0 | 1 | 1 |
| 15 | 1 | 0 | 1 | 0 | 1 | 0 | 51 | 0 | 1 | 0 | 1 | 0 | 0 |
| 16 | 1 | 0 | 1 | 0 | 1 | 1 | 52 | 0 | 1 | 1 | 0 | 0 | 0 |
| 17 | 1 | 0 | 1 | 1 | 0 | 1 | 53 | 0 | 1 | 1 | 1 | 0 | 0 |
| 18 | 1 | 0 | 1 | 1 | 1 | 0 | 54 | 1 | 0 | 0 | 1 | 0 | 0 |
| 19 | 1 | 0 | 1 | 1 | 1 | 1 | 55 | 1 | 0 | 1 | 0 | 0 | 0 |
| 21 | 1 | 1 | 0 | 1 | 0 | 1 | 56 | 1 | 0 | 1 | 1 | 0 | 0 |
| 22 | 1 | 1 | 0 | 1 | 1 | 0 | 57 | 1 | 1 | 0 | 1 | 0 | 0 |
| 23 | 1 | 1 | 0 | 1 | 1 | 1 | 58 | 1 | 1 | 1 | 0 | 0 | 0 |
| 24 | 1 | 1 | 1 | 0 | 0 | 1 | 59 | 1 | 1 | 1 | 1 | 0 | 0 |
| 25 | 1 | 1 | 1 | 0 | 1 | 0 | 61 | 0 | 0 | 0 | 0 | 0 | 1 |
| 26 | 1 | 1 | 1 | 0 | 1 | 1 | 62 | 0 | 0 | 0 | 0 | 1 | 0 |
| 27 | 1 | 1 | 1 | 1 | 0 | 1 | 63 | 0 | 0 | 0 | 0 | 1 | 1 |
| 28 | 1 | 1 | 1 | 1 | 1 | 0 | 64 | 0 | 0 | 0 | 1 | 0 | 0 |
| 29 | 1 | 1 | 1 | 1 | 1 | 1 | 65 | 0 | 0 | 1 | 0 | 0 | 0 |
| 31 | 0 | 0 | 0 | 1 | 0 | 1 | 66 | 0 | 0 | 1 | 1 | 0 | 0 |
| 32 | 0 | 0 | 0 | 1 | 1 | 0 | 67 | 0 | 1 | 0 | 0 | 0 | 0 |
| 33 | 0 | 0 | 0 | 1 | 1 | 1 | 68 | 1 | 0 | 0 | 0 | 0 | 0 |
| 34 | 0 | 0 | 1 | 0 | 0 | 1 | 69 | 1 | 1 | 0 | 0 | 0 | 0 |
| 35 | 0 | 0 | 1 | 0 | 1 | 0 | 71 | 0 | 0 | 0 | 0 | 0 | 0 |

2-17. VCXO 1A1A1. (fig. 6-4)

*a.* The VCXO may be modulated from three sources: a 1-kHz internal oscillator, external modulation, or the actual data word itself. All three of these signals, after being subjected to their respective controls, will appear at TP2 as the analog or digital modulation signal to the 21.4 MHz IF frequency oscillator.

(1) A 1-kHz internal modulator is formed by U1–A, U1–B, R43–R46, R48, C21 and C29. When the positive 1-kHz GATE signal from MODE CONTROL III module is applied to J1–6, gate transistor U1–C is biased on. With U1–C turned on, ground is applied to the common emitters of U1–B and U1–A, permitting the 1-kHz oscillator to begin oscillation. When U1–A is biased on, ground is applied to C29 through U1–A causing it to discharge. This places a bias voltage on U1–B which holds it turned off. Then C20 charges through U1–A and R45 until a positive voltage is reached which is sufficient to turn on U1–B. When U1–B turns on, C21 is discharged and turns U1–A off. Then C21 charges through U1–B and R48 until U1–A becomes biased on again, thus completing one cycle of oscillation. The output of the oscillator is coupled through limiting resistor R10 to the base of Q6. Resistors R9 and R11 form a bias network and C22 is used for pulse shaping.

(2) The signal which turned on U1–C to start the 1-kHz oscillator also turns on gate transistor U1–D. With U1–D on, a ground is provided for Q6 through R18. Emitter and collector resistors, R18 and R37 respectively, are equal in value, therefore the output is a 1-kHz signal swinging about half the supply voltage, or 5 volts. This 1-kHz signal is coupled through C28 to the base of Q8.

(3) External modulation may be utilized by injecting a 10 Hz to 20-kHz signal at front panel connector EXT MOD IN. When the MODE switch S7 is in the EXT position a logic one level EXT MOD GATE is present at J1–14. This logic one level, through R21, biases on gate transistor U1–E which provides a ground through R20 to the emitter of Q7. With an external modulation signal applied to J1–3 and coupled through C16, Q7 will gate this signal through as long as the EXT MOD GATE signal is present. The output of Q7, like that of Q6, will also swing about 5 volts and be coupled through C28 to the base of Q8.

(4) Resistors R25, R26, R29, R30 and transistor Q8 form an amplifier with a gain of approximately two. The modulating signal, either internal (1 kHz) or external, is amplified and coupled through C27 to the gate of Q9. Resistors R36, R38 and transistor Q9 are used as a source follower to present a low impedance to DEVIATION potentiometer (R1) located on the front panel. The modulation signal is coupled through C20 to the DEVIATION pot (R1) which controls signal amplitude and returns the signal to the VCXO at J1–5 (VAR DEVIATION). This signal is routed to the gate of another source follower (Q11 and R39) to prevent loading effects to the potentiometer. This signal is coupled through C26 and R33 to one input at U2, pin 2. Pin 2 is also the input point for data modulation.

(5) Data modulation and the DATA GATE signal come from MODE CONTROL III module. These two signals are called VCXO B and VCXO C respectively. When no data is present at J1–2, the logic level is zero and Q14 is biased off. At this same time, VCXO C at J1–12 will be logic

one, causing Q5 to be biased on and provide a ground to the voltage divider network R31 and R59. The low deviation clamp circuit Q13, R5, R16 and CR1 and wiper of variable resistor R59 are connected to R57. The low deviation is adjusted by variable resistor R5 and CR1 is used to track the emitter-base junction of Q13 for temperature stability. The voltage on the emitter of Q13 is then the upper limit of the voltage swing at R57. Resistor R57 and capacitor C23 are used to shape the incoming pulses to simulate the actual operation of the remote transmitters.

(6) If data were present, the VCXO C line is logic zero turning Q5 off and permitting Q14 to present the data to R57. When the data level is low the deviation is low; when the data is high the deviation is high. Data input then passes through R24, the high deviation adjust, and arrives at U2 pin 2 as does internal or external modulation when selected. The summing point for both digital and analog modulation signals is U2 pin 2 (TP4).

(7) Operational amplifier (U2), is used as a variable gain device which will transfer the modulation signal to the crystal oscillator. The noninverting input of U2 pin 3 is clamped to approximately 5 volts to provide a reference level for incoming signals. Variable resistor R7 is the offset null adjustment which permits the operational amplifier to be correctly balanced. The feedback loop for U2 (R32, R49, R60) can be two values, determined by the signal at J1–4 which comes from the front panel FSK switch (S8). When the FSK switch is in a wide deviation position J1–4 will be high, turning on Q15 and effectively removing R49 and R32 from the feedback loop. When a narrow deviation is selected, Q15 is turned off and the two 10 k ohm series resistors, R49 and R39 now parallel to the 20 k ohm, R60 and reduce the network resistance to 10 k ohm, halving the circuit gain. Reduction in gain reduces the output swing of U2, therefore reducing the amount of deviation. Narrow deviation is ±1.5 kHz and wide deviation is ±3 kHz. The output of U2 at pin 6 is the analog or digital modulation signal to the crystal oscillator (TP2). This signal also drives the gate of the source follower Q12 and R53, used to keep the loading effects on U2 low. The resistor in the source leg of Q12, R53, is selected in test to provide the correct gain to the amplifier stage Q16, R51, R52, and R54. The amplified modulation signal is routed to J1–10, then to the DETECTOR-OUTPUT module.

*b.* After the analog or digital modulation has undergone its gating and is amplified, it is now injected into the crystal oscillator which generates the 21.4-MHz IF frequency. The crystal oscillator is composed of the following circuit elements:
Y1, R1, R3, R6, R22, R23, R28, C1–C4, C6–C9, L1–L3, L5, L8, Q1, Q2, CR4 and VR9

Not all of these components are required for the design of the basic oscillator, some are used for various related functions such as temperature compensation, filtering, etc, and are therefore included with the oscillator.

(1) The oscillator is the Butler configuration, with its main frequency control element being the series resonant crystal Y1. The natural resonant frequency of Y1 is 21.394 MHz and is pulled to the 21.4-MHz IF frequency by its associated components. Diode VR9 is a varactor diode, or a diode whose capacitance may be altered according to the bias voltage applied to it. The modulating signal from U2 pin 6, after passing through the RF decouping network C11 and L4, becomes one of the biasing signals causing VR9 to vary its capacitance. This modulation, in effect changes the resonant frequency of Y1 which causes the deviation changes in the IF frequency.

(2) For the oscillator to operate, a positive going signal must be present at J1–13, the VCXO GATE from the MODE CONTROL III module. When turned on, the oscillator will not come up to its full output immediately so this VCXO gate signal will appear prior to the modulating signal by two specified times. The time the oscillator is gated on prior to the modulation signal is known as the guard band and will be 15 ms ±ms for W/S modulation (75 Hz) and 5 ms ±2 ms for W/F modulation (300 Hz). The VCXO gate, when positive, biases on Q3 which provides a ground path through R3 to the emitter of Q1. Transistor Q1 then turns on, at this time its output is only low amplitude noise. From the collector of Q1, the noise signal is passed through coupling capacitor C6 to the base of Q2. From the emitter of Q2, this noise is injected into crystal Y1. Crystal Y1 acts as a filter and passes only the frequency to which it has been biased, this being the center frequency of 21.4 MHz at initial turn on time. The crystal output is then coupled through VR9 and decoupling capacitor C8 to the emitter of Q1 where it is now amplified and sent back through the loop. Inductor L1 and C3 with trimmer capacitor C4 form the tank cir-

cuit of the oscillator that will provide the necessary 360° phase shift needed for oscillation. The oscillator then reaches its full amplitude of output at center frequency before the modulating signal is present. Inductor L5, in parallel with Y1, is used to tune out the crystal holder capacitance. Variable resistor R6, through the decoupling choke L2, provides an adjustable bias to VR9 that may be adjusted to 21.4 MHz, the center frequency. Diode CR1 is used to track the emitter-base junction of Q1. Zener diode VR5 maintains a constant bias voltage over the temperature range of the equipment. The bias voltage that is felt on the base of Q1 is coupled through the RF decoupling network C7 and L3 to the base of Q2. Additional RF decoupling is provided by C2, C1, L8 and C9

(3) The signal from the oscillator is tapped at the base of Q2 through capacitor C12 and is amplified by IF amplifier Q4, R40 and R41. The IF frequency is routed into the double tuned tank circuit of C14, C15, C17–C19, L6, L7 and L10. Trimmer capacitor C15 in parallel with padding capacitor C14, permits the tank circuit to be tuned to peak output at the IF frequency. Three inductors (L6, L7 and L10) form a *Tee* equivalent to a RF transformer. Capacitors C17, C18, and C19 remove harmonics from the tank circuit The overall effect of the double tuned tank is to take an output of approximately 2 k ohms and bring it to the desired output impedance of 50 ohms. The output of the double tuned tank receives further impedance matching from the $\pi$ pad R15, R34 and R35. The IF frequency is routed to J2 then to RF MIXER/AMPLIFIER

## 2-18. Detector-Output 1A1A2 (fig. 6-5)

*a.* Front panel METER SWITCH S10 will determine if front panel meter M1 indicates either DEVIATION level or RF level. When S10 is in the DEV position, J1-2 receives a deviation signal from J1-10 of the VCXO module This signal can be the result of either internal modulation (1 kHz), external modulation (10 Hz to 20 kHz) or digital modulation. To properly calibrate the meter, the modulation must be from an external source; thereafter the meter may be used to monitor the signal level of all types of modulation.

*b.* In a no signal condition, a bias of 4.2 volts is established on U1-A's base by the bias network, R2 and R3. Coil L2 and capacitor C7, both in the B + supply line, are used for RF decoupling and do not affect the dc bias levels. The deviation input signal is left on the base of U1-A through C4, used for dc isolation. Transistor U1-A and resistor R4 form an emitter-follower circuit with filtering being by C9. Meter M1 must be able to display a steady meter indication even at the lower limit of the external modulating signal (10 Hz), therefore large values of capacitance are used as filters by U1-A and U1-B. The signal from the emitter of U1-A is felt on the base of U1-B, another emitter follower. Transistor U1-B and resistor R8 form an emitter follower which presents a high impedance to the output while C13 parallels R8 for additional signal filtering. This signal is sent to J1-13 through R14, a potentiometer which may be used to set the drive current to meter M1.

*c.* It may now be noted that the meter connected to J1-12 is driven by circuit U1-C, U1-D, R13, R16, R24, R25, C19, and C22. This circuit is identical to the circuit just described above. Variations in circuit output due to temperature changes will affect both sides of the meter drive circuits equally, producing compensations which will maintain meter zero over wide temperature changes. The additional of R26, R27 and C27 to the temperature compensation circuit is an additional compensation for leakage current. Test points TP4 and TP5 may be used as connection points for the attachment of an external meter when performing module adjustments. Variable resistor R7 is the meter zero adjustment which changes the bias voltage on the base of both U1-A and U1-C to balance the output of both meter drive circuits. Meter zero is adjusted with no signal input while, R14 is adjusted with a 3-kHz signal of known amplitude as an input.

*d.* RF level is also read on the front panel meter M1. The RF input from the RF MIXER/AMPLIFIER module at J2 is coupled through DC blocking capacitor C30 to transformer T1. Transformer T1, along with C6, C8 and VR1, form a one pole voltage tuned tracking filter whose function is to filter out all frequencies other than the selected center frequency. Tuning voltage, from the channel number resistor string, is present at J1-3. Passing through RF decoupling network L1 and C3 and current limiting resistor R1, this tuning voltage will bias varactor diode VR1. As this tuning voltage is stepped through its 9 voltages, ranging from 1.28 to 7.08 volts, the varactor diode VR1 will modify the resonant frequency of the filter to produce 9 tuning bands, each approximately 2 MHz wide

The lower limit of the filter is 160.062 MHz and the upper limit is 176.862 MHz with some overlapping of the bands. Range trimming capacitor C6 permits precise bandpass adjustment to the center frequency. This filter performs an additional function of changing the signal from a 50-ohm input impedance to approximately a 2 k ohm output impedance.

*e.* The B+ at J1–1 receives RF decoupling from two ferrite glass bead filters, Z12 and Z13, and line filtering from C1. This voltage then is divided by R5 and R6 to become the gate bias voltage to gate 2 (pin 2) of Q1. Similarly, R38 and R39 form another voltage divider through T1, which provides gate bias to gate 1 (pin 3) of Q1. Capacitors C11 and C31 are RF bypass capacitors. Bias networks along with Q1, R9 and T2, form a RF amplifier. This RF amplification is necessary to compensate for signal losses which will occur due to necessary filtering and signal conditioning. The source resistor for Q1 is R9 and is selected in test for a specified current range (about 8 to 10 ma) which will give the correct amplifier gain. The signal on pin 3 of Q1 (gate 1) is amplified and applied to the load transformer T2 which, through L3, is the path to J3. Choke L3 is used for RF decoupling and C12 and C14 are RF bypass capacitors. Capacitor C13 permits this amplifier to be tuned to the middle of the band. Transformer T2 changes the impedance of the signal from approximately 2 k ohm to 25 ohms. The RF input signal at J2 was at −10 dbm level and the output at J3 should be the same. In order to achieve this, a pad R11, R16 and R17 is used. This pad is selected in test to give a −10 dbm output at J3 which goes to the front panel attenuator switches.

*f.* The signal developed by the RF amplifier routed to the attenuator and filter string, is also routed to an RF detector. The actual signal rectification is done by CR3 with the additional components used to provide temperature compensation and precision control to the signal as displayed on meter M1.

*g.* The RF frequency is presented to the junction of CR3 and R40 through dc blocking capacitor C18. Resistor R40 is used as line termination resistor and CR3 rectifies the signal and places it on the inverting input of operational amplifier U2. CR3 and CR4 are both "hot carrier diodes" which are used because of their efficiency at high frequencies. The purpose of CR4 is to track CR3 to maintain temperature stability. Capacitors C20, C21, C24, C26 and C29 are RF bypass capacitors and L6 is used for RF decoupling. A reference voltage to the noninverting input of U2 (pin 3) is established by the divider made up of R20, R21, R30, R23, and R19. Resistor R19 is adjusted to set meter zero with no input signal; R36 in the line between R19's wiper and U2–3 balances the resistance used in the negative feedback loop (R34, R35) to maintain thermal stability of the circuit. The output of U2–6, the detected and amplified RF signal, is routed back to the inverting input of U2–2. Resistors R35 and R34 function as a gain controlling device. The output of U2–6 now pass through ferrite beads Z10 and Z11, RF decouplers, to meter M1 (provided meter switch S10 is in the RF LEVEL position), through M1, back through two more ferrite bead RF decouplers Z9 and Z8, and through R29 and R37 to the voltage divider network of R21 and R30. Resistor R28 is used to shunt the meter which has a 100 microamp movement. Resistor R29 is adjustable to allow the meter to be calibrated to the POWER SET mark and R37 provides current limiting even though R29 is adjusted fully cw. Test points TP1 and TP2 may be used as connection points for the attachment of an external meter when performing module adjustments.

## 2-19. Loop Filter/VCO 1A1A3 (fig. 6-6)

*a.* The Loop Filter/VCO consists of a sample-and-hold phase detector, a frequency detector, an operational integrator, a voltage controlled oscillator, and two buffers.

*b.* Coarse frequency control required to assist the phase lock circuit when changing channels or applying power, is supplied by the frequency detector. A strobe pulse from the Programable Divider module is applied to J1–5. This pulse is negative going and is approximately 250 nsec wide at the 2-volt level. Capacitor C1 is a dc blocking capacitor and the combination of R1 and R3 form a divider network providing an offset bias voltage to U1–C pin 5. The positive going strobe pulse at U1–C pin 4 is the input to inverter stage U1–D and may be monitored at TP 3. This pulse, after being double inverted and buffered by gates U1–A and U1–B, is applied to the base of Q1. Transistor Q1 is normally cut off but during strobe time it is driven into saturation, discharging C4. At the end of strobe time, C4 begins charging through R9 and R8, beginning the monostable cycle of oscillator U2-A.

U2–B, C4, R8, R9. When C4 has charged to the threshold voltage of U2–B pin 8, U2–B pin 10 will go low causing U2–A pin 4 to go high. These logic conditions remain unchanged until another strobe pulse arrives to discharge C4. The duty cycle of this monostable multivibrator may be changed by variations in the strobe interval time or by manual adjustment of R8 (R8 is an internal adjustment only and is preset during module alinement). The monostable multivibrator output at U2–B pin 10 is buffered and inverted by U2–C and may be monitored at TP7. This is one of the two inputs to the loop filter.

*c.* The loop filter is an operational integrator whose function is to integrate and smooth the output from the frequency detector and the sample-and-hold phase detector. The loop filter consists of U3, R16, -R20, and C7–C9. The inverting input to the operational integrator (U3–3) will see the summation of signals from the frequency detector (through R14 and R18), and the phase detector (through R15) The higher the voltage at U3–3, the lower the output will be at U3–12. Components R17, R19, C7 and C8 are used as phase compensation networks. The noninverting input (U3–4) sees a dc reference level through R16 from the divider network R36 and R37. Capacitors C27, C30 and C32 add filtering to this bias line for dc voltage stability. The feedback loop and time-constant control for U3 is C9 and R18. The output of the loop filter contains small, but detectable spikes at the reference frequency (6.25 kHz) which may be monitored at TP5. Resistor R21 and capacitor C10 filter these spikes and provide a smooth VCO control voltage.

*d.* The VCO is a modified Colpitts oscillator consisting of Q9, L1, C11–C13, C15, VR2, VR3, and R26. The junction field effect transistor (Q9) provides a high degree of short-term stability. L1, C15 and varactor diodes VR2 and VR3 comprise the tank circuit. The signal from the loop filter, after passing through isolation resistor R22, is felt on the anode of varactor diode VR2. The cathode side of VR2 receives a dc reference bias from the divider network formed by R40 and R41. The 7.08 vdc tuning voltage is applied to J1–6 while this same voltage is divided down to a lower value by the channel select switches and then applied to J1–4 (nine tuning steps ranging from 1.28 vdc to 7.08 vdc may be selected). With both ends of the divider (R40, R41) having 7.08 vdc as their original source, any variations in voltage due to temperature fluctuations is equally felt by both resistors, the net effect being excellent temperature stability of the varactor's bias voltage. The tuning voltage at J1–4 is felt on the cathode of VR3 through isolation resistor R24 while the anode of VR3 reaches ground through L1. As the capacitance of either or both for the varactors decreases the oscillator frequency increases; conversely, increases in capacitance decrease frequency.

*e.* A typical example in which the frequency detector, loop filter, and VCO operate to correct a frequency error Assume there exists a frequency out of the VCO which is too high, the result will be that strobe pulses from the Programable Divider (1A1A5) will occur at shorter time intervals than they should be. This will cause the output of the monostable multivibrator at U2–B pin 10 to change its duty cycle such that its off time decreases in relationship to its on time. After being inverted by U2–C, the signal monitored at TP7 will show a signal whose duty cycle has been increased in favor of its low state. The lower the voltage on the input to U3 the higher will be its output voltage which causes the back-bias on VR2 to be decreased. Reducing the back-bias on VR2 will cause an increase in capacitance which in turn lowers the output of the VCO to correct for its too-high frequency output. This same type of correction will occur with inputs from the sample-and-hold phase detector.

*f.* Fine tuning frequency control is supplied by the sample-and-hold phase detector which consists of components Q3–Q5, Q7, Q8, U2–D, R2 R4, R6, R11–R13, CR1, C2, C3, C5, and C6 The 6.25-kHz reference frequency from the programable divider is differentiated by C2 and R2 The positive going spike is shunted to B+ by CR1. Gate U2–D inverts this now narrow pulse and applies it to the base of Q3. Transistor Q3 momentarily saturates once for each cycle of the reference, discharging C3 for a very short period. When Q3 is turned off, C3 will charge through R4 and R6, producing a positive going ramp voltage which rises from zero to approximately 3 volts. This ramp voltage signal can be conitored at TP2. The ramp cycle is repeated once for each reference cycle. The strobe pulse at U1–D pin 12 is inverted and causes Q6 to turn on for approximately 250 nsec. This signal in turn, will permit the bilateral gate (Q4, Q5 to sample the ramp voltage and charge or discharge C5 to match the voltage across C3. The ramp voltage may be either greater or less tha

voltage on C5 at strobe time, the bilateral gate is needed to permit current to flow in either direction. Transistors Q7 and Q8 are connected as a DC amplifier with gain control (gain of 2) being set by R11 and R12. This amplifier also provides a high impedance load to C5. The amplified signal is decoupled by C6 and becomes the second input to the loop filter through R13 and R15.

*g.* The VCO output is coupled through C17 to two buffers, one for each output. The operation of both buffers is identical so only one will be described. Decoupling capacitor C19 applies the VCO output (local oscillator frequency) to the base of Q11 which is biased as a class A amplifier by R29 and R33. Resistor R33 acts as a current limiter and C24 as a RF bypass. Transformer T2 is a wideband type which reduces the impedance to the output at J3 to about 50 ohms for line matching. Capacitor C23 is for RF decoupling while C26 is a DC blocking capacitor. The LO frequency is output to the synthesizer/mixer (1A1A4–J5). This buffer receives isolation and RF bypass on its B+ line from L2. The other buffer stage (Q10, T1, R27, R28, and R32) differs only in having TP6 available to monitor the LO frequency with isolation supplied by R35. This buffer outputs to the RF amplifier/mixer (1A1A7–J2).

## 2-20. Synthesizer/Mixer 1A1A4 (fig. 6-7)

*a.* The Synthesizer/Mixer can be broken down into six major areas: two mixer stages, two filter stages, an amplifier stage, and a buffer.

*b.* Mixer number one is made up of components Q1, Q2, C10, C12, C13, C14, C18, R1–R3, R5–R11, L4 and T1. The 90-MHz reference frequency from the Reference Generator is injected into the mixer at J4 and coupled through C10 to the base of Q1. The input at J5 is 138.725 MHz to 154.4625 MHz from the loop filter/VCO. After this signal is attenuated by the *pi* pad R1, R2 and R3 (50-ohm termination), it is coupled through C13 to the base of Q2. Capacitor C12 couples the output of Q1 into Q2 and C14 takes the Q2 output and couples it into Q1. The bias network for Q1 is made up of R5 and R6 while R9 is the emitter load resistor; biasing for Q2 is R7 and R8 with R10 the emitter load resistor. Transistor Q1 and Q2 will both have 90 MHz and the VCO frequency as signal inputs. Transistors Q1 and Q2 have their collectors tied to each other and develop their output signals across transformer T1. Inductor L4 and capacitor C18 are used for decoupling and R11 parallel the T1 secondary as a load resistor.

*c.* The signal at the primary of transformer T1 is both the sum and the difference frequencies resulting from mixing 90 MHz with the VCO frequency. To obtain only the difference frequency, a 2-pole filter is used (T1, C5, C6, C22, C24, L5, VR2, VR4, T2, R16 and R17). The first filter pole is the primary of T1 and components C6, C22, and VR2. Resistor R16 supplies isolation for the tuning voltage input to VR2, a varactor diode. Capacitor C6 is adjusted for proper filter tracking. Inductor L5 is for inductive coupling between the two filter poles. Varactor VR4, and capacitors C5, V24 and the primary T2 make up pole number two. As tuning voltage is increased from 1.28 volt to 7.08 volts, the back-bias on VR2 and VR4 is increased causing their capacitance to decrease, thus tuning the 2-pole filter to a higher bandpass. The bandpass of this filter is 1 db down from the point of maximum transmission at 1.9 MHz to 64.6425 MHz and is one of the two inputs to the second mixer.

*d.* A cascade amplifier is made up of components U1, L1–L3, C7, C9, C11, C15, C16, and R4. The spectrum input from the reference generator at J2 passes through a high-pass filter C7, C9 and L1 which removes the low frequency spectrum energy that would otherwise saturate U1. Resistor R4 is the input bias resistor for U1. Capacitors C11, C15, C16, C17 are part of the compensation network needed for correct frequency response. Inductor L3 is a choke used for RF decoupling.

*e.* The output of U1–6 routes to a voltage-tuned 4-pole filter which reflects only one spectrum line and rejects all others. Each pole is listed below.

*Pole 1.* C1, C19, L2, VR1, R13
*Pole 2.* C2, C21, L6, VR3, R14
*Pole 3* C3, C26, L7, VR5, R19
*Pole 4.* C4, C33, primary of T3, VR6, R20

Capacitor C20 couples poles 1 and 2; C25 couples poles 2 and 3; C28 couples poles 3 and 4. As tuning voltage is increased, the frequency selected increases as it did with the two-pole filter. The output of this filter (46.875 MHz to 61.875 MHz) is monitored at TP1 and is the second input of mixer number 2.

*f.* Tuning voltage from the channel selected

switch resistor string at J1-4 is buffered by Q3, R12, and R15 with C23 and C27 acting as decoupling capacitors. This buffered tuning voltage is applied simultaneously to both the 2- and 4-pole filters.

*g.* Mixer number two is made up of components Q4, Q5, C29–C32, R21–R26, L8 and L9. The operation of this mixer is the same as the operation of the first mixer (para 2–20*b*). The input from the 2-pole filter is monitored at TP2. The output of the second mixer now goes to amplifier U2 which will amplify the difference frequency The output of U2 drives wideband transformer (T4) which changes the impedance from 2 kilo-ohms down to a 50-ohm output at J3. Capacitors C37, C38 and C39 are part of the U2 compensation network while C35 and C36 are used for decoupling The output of the second mixer ranges from 1.85625 MHz to 3.7125 MHz and is the input to the Programable Divider.

## 2-21. Programmable Divider (fig. 6-8)

*a.* The Programable Divider contains five major sections: an amplifier/shaper, a counter, a monostable multivibrator, a diode matrix and a divide-by-three counter.

*b* The Synthesizer/Mixer routes a frequency of 1.85625 MHz to 3.7125 MHz, depending upon the channel selected, to J3. Transformer T1 transforms the 50-ohm input to about 200-ohm output. This signal is then coupled through C3 to the input of amplifier U3. Resistor R6 is the input balancing resistor and C4 provides AC ground to the input. The output of U3 receives pullup assistance from R9 and is then coupled through C6 to the base of Q1. Diode CR5 removes negative going excursions from the input by shunting them to ground. Additional amplification and shaping is done by Q1 with R16 being its collector load resistor. The input signal has now been given faster rise and all times suitable for use by the counters and is viewed at TP1.

*c* The counter, or programable divider section, consists of components U1, U5, U7, CR1–CR4, CR6, CR7, C9, R7, R8, R12–R15, R18 and R19. The counter elements U1, U5, and U7 are binary-coded-decimal counter/storage elements that are wired in biquinary mode. The counting operation is performed on the falling (negative-going) edge of the input clock pulse. By using the front panel channel select switches, the counter stages may be programed to divide by any number from 296 to 595. Each clock pulse at U7 pin 12 will clock U7 one additional count every two words. Pin 2 of U7 will go low on the next count and advance U5 one count. Ten clock pulses are required to advance U7 one complete count cycle and one-hundred counts are therefore needed to advance U5 one complete count cycle. Every two words U5 pin 2 goes low, U1 is advanced one count. Integrated circuit U1 is the hundreds count, U5 the tens counter, and U7 the units counter. Diodes CR1–CR4, CR6 and CR7 determine the maximum count of these counters by *anding* together various count stages and permitting a strobe pulse to be generated which preset the counters. CR1 takes the 4-bit output of U1 and *ands* it with the 1-bit, making a count of 500; this information is *anded* with the 8-bit (CR3) and the 2-bit (CR4) from U5, the tens counter, which now gives an *anded* signal for the count 590; the units counter, U7 takes the 4-bit (CR6) and the 1-bit (CR7) and adds this count giving an output at the count of 595. Capacitor C9 parallels CR7 to speed up the last count output by bypassing CR7. When the above-mentioned outputs are all high, a strobe start pulse is generated. When the strobe pulse is at the 0 logic level, the information on the preset gates is transferred to the outputs, removing the strobe start pulse. The next clock to arrive at U7 pin 12 will, again, begin the count sequence. Resistors R7, R8, R12–R15, R18 and R19 are pullup resistors which hold their respective inputs high until a 0 logic level is applied externally from the channel select switches.

*d.* When the maximum count has been reached by the Programable Divider a logic 1 signal is coupled through speedup capacitor C7 to the base of Q2. Components Q3, Q4, CR11, CR12, R22, R24, R27 and C8 form a monostable multivibrator. The positive signal on the base of Q2 causes it to conduct and place a low signal, through R24, on the base of Q4. Transistor Q4 conducts and applies a high on the base of Q3 which turns on, applying a low through R22 and R24 to the base of Q4 causing a *latch* condition. This condition will remain until C8 charges up through R25 and R26 and causes Q3 to turn off, (approximately 220 nsec). This has generated a negative going strobe pulse which will permit the Programable Divider to preset input data to the outputs.

*e.* The diode matrices U2, U3 and U4, consist of three individual diode matrices with some of their internal fusible links, intensionally blown out (see figure 6–8). If any one of the input lines (pins 2, 3, 4, 5, 6, 9, 10, 11, 12, 13) has a logic

zero applied from the front panel select switches, an appropriate output line (pin 7 or 8) will go low. This becomes an input to the programable divider. Resistors R3–R5, R10, R11 and R17 are output pullup resistors.

*f.* The divide-by-three counter is made up of components U8, CR9, CR10 and R23. A frequency of 18.75 kHz at J2, which originated at the Reference Generator module, is applied to the clock inputs of both U8A and U8B. On the rising edge of the clock pulse, the logic level present on the data line is transferred to the Q output, with Q reflecting the opposite logic condition. The use of CR9 and CR10 causes the output states of U8A and U8B to be repeated with every third clock pulse in, so U8B pin 13 represents 6.25 kHz. This is routed from J2–8 to the loop filter

## 2-22. Mode Control I 1A1A6 (fig. 6-9)

*a.* Mode Control I module receives information from the front panel MODE switch (S7) which is inverted by the four gates of U2 and then used to control certain timing functions. REP–A (J1–4), REP–M (J1–15), SEQ–A (J1–5), and SEQ–M (J1–6) are applied to gates U2D, U2B, U2A and U2C respectively. With one leg of each of these gates grounded the gates act as inverters. When a switch position is selected a logic one is placed on the input to the gate; when a gate is not selected, pulldown resistor R1–R4, will maintain a low on the input to its gate. The output of the selected gate is logic zero while all the other outputs are logic ones. The four gates of U8 receives signals called $\overline{\text{SEQ–M}}$, $\overline{\text{REP–M}}$, $\overline{\text{REP–A}}$ and $\overline{\text{SEQ–A}}$ as well as having a common leg of all four gates tied together. Should any of the four inputs to U1B (Audio Gate J1–20, M Mode Inhibit J1–10, Burst Generator Gate J1–22 or $\overline{\text{Activate Synchronizer}}$ J1–16) be in a logic one condition, an inhibit signal is present. These signals are gated by U1B and inverted by U5D, placing logic one on the common line to U8 when this inhibit condition is present. Under an inhibit condition, all the outputs of U8 are logic zero; when the inhibit is not present, the gate selected will have its output logic one. The signal Activate Synchronizer is normally logic one, but when the START button (S11) is pressed a negative going pulse is seen at U1B–9; this in turn will gate on the selected mode for the duration of the pulse (833 $\mu$s). Should either of the manual modes have been selected, U1A–1 will generate a negative going pulse which will become the $\overline{\text{Load}}$ signal (TP2) to Mode Control II. In addition, either of the modes will, when the START button (S11) is pressed, cause a negative pulse at U10A–3 and, after being inverted by U10B, this positive pulse is the signal Dump M (TP1) to Mode Control II.

*b.* The same switch information, as presented to the four gates of U2 will be NOR'd together by U3A. The resultant output signal from U3A–1 is utilized by the reset synchronizer circuit (fig. 2–22 and 2–23). The purpose of the reset synchronizer is to generate a reset pulse synchronous with a 600-Hz signal (2 x fast) whenever a mode change is made. This pulse will also have a duration equal to one half of the 600 Hz input (833 $\mu$s). If no logic zero signal is present at the Repetitive Selector Inhibit input (J1–23), a mode change through SEQ–A, SEQ–M, REP–A or REP–M will produce a positive pulse at U3A–1 (in between switch positions). Consider the sequence of events concerned with pulse 1 on Timing Diagram (fig. 2–22) and Reset Synchronizer schematic (fig. 2–23). This pulse at point D will cause flip-flop U7A/U7D to latch with point G at a logic zero. At this time, point E is already logic zero, so point H will go to logic one. This logic one will hold point K to logic zero and cause point I to logic zero. When pulse D returns to logic zero state, all three inputs to U4A (C, D, I) will be logic zero causing point J to go to logic one. This moves point F to logic zero, point B is now logic one and no further action takes place. When point B does go to logic zero, the output of flip-flop U7B/U7C, point E, will go to logic one. This logic one moves point H to logic zero and, with point F already logic zero, point K will go to logic one and point L to logic zero. When point H went to logic zero, point I was forced to logic one, blocking any further inputs to gate U4A. When point B again changes state to the logic one condition, point E will go to logic zero and with point J now logic zero, the output of U7B point F changes to a logic one state. This logic one causes point K to go to logic zero and point L to go to logic one, producing the synchronous reset pulse.

*c.* The reset pulse is applied to the common line to all four gates of U6 which NOR the mode inputs and the reset pulse. All the outputs of U6 are NOR'd by U3B and inverted by U9A. The positive going reset pulse is now present at U4B 13, which has two additional inputs. One of the inputs, U4B–11, is a positive-going (833 $\mu$s) pulse from the START (S11) button if the SEQ–A

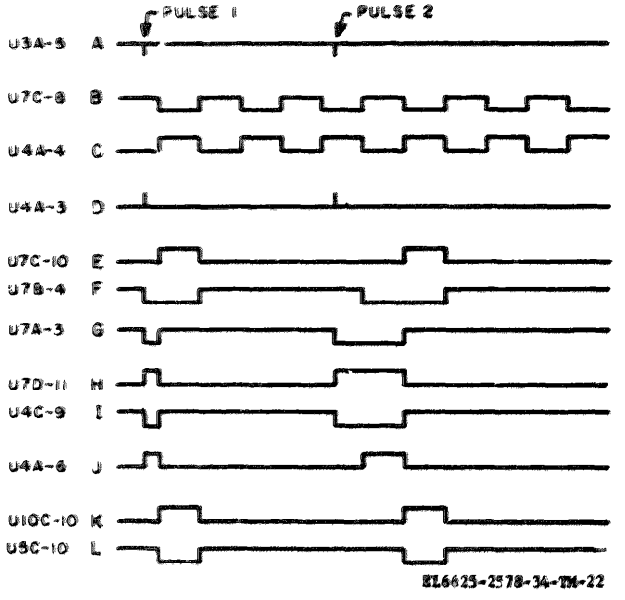



Figure 2-22. Reset synchronizer timing diagram.

mode is selected. The other input U4B–12 is the POWER ON reset pulse at J1–19. Any of the three inputs will cause U4B–10 to generate a negative-going pulse which is inverted by U9D and then applied to U9B–5, output J1–21 (burst generator reset), and U12C–8. U9B will NOR this reset/start pulse with the end of cycle reset signal from Encoder II Inverter U5B inverts this negative-going pulse and the subsequent positive pulse is a reset to flip-flops U14A and U14B (TP3) and the output signal to J1–13 (reset). A reset signal at power turn-on, mode change, end of cycle, and sequence initiate has been generated.

*d.* The positive going reset/start pulse at U12C pin 9 becomes a negative going pulse at U12C–10 which is inverted by U12D to become a reset to flop-flips, U11A and U11B. This places U11A–2 at logic one. When a SEQ–A Initiate pulse arrives from Encoder II module (J1–26) it clocks U11A causing U11A–1 to go to logic one; at the positive-going edge of the 300-Hz signal, fast (J1–17), U11B will clock this logic one to its output U11B–13. This logic one forces U12A–3 to logic zero and this signal is then inverter by U13A to become a logic one at U12C–9, the other input to the reset NOR gate U12C. This signal will reset U11A and U11B. When the positive edge of the signal $\overline{2 \times \text{fast}}$ (J1–11) arrives at U12B–6, the output U12B–4 will go to logic zero. Since U11B has already been reset both U12A–1 and U12A–2 are now at logic zero, forcing U12A–3 to logic one. This has reset the system described and also generated a positive-going clock pulse to U14B–11 which is synchronous to the 300-Hz input.

*e.* The clock pulse to U14B–11 causes U14B–12 to go to logic zero; when the negative going signal $\overline{\text{End Word}}$ (J1–14) arrives at U15B–5, the output U15B–4 goes to logic one. This causes U13D–11 to go to logic zero, U13C–10 to go to logic one, and U1A–1 to generate a negative going $\overline{\text{Load}}$ pulse at TP2. U13C–10 also moves U13B–4 to go to logic zero and this pulse is inverted by U5A to become a positive pulse at J1–7 (Dump to Mode Control II). This pulse is viewed at TP4.

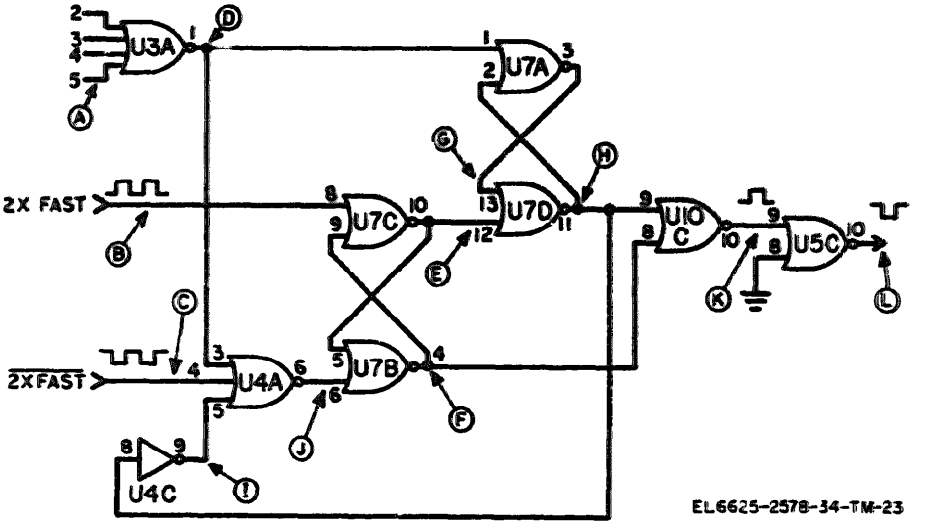



Figure 2-23. Reset synchronizer schematic.

*f.* Had the MODE select switch (S7) been in REP-A, START button (S11) would have caused a clock pulse to be generated and applied to both U14A-3 and U15D-13. This would cause U15D to go to logic one and make both a Load (TP2) pulse and a Dump (TP4) pulse. The pulse to U14A-3 would have made U14A-2 logic zero and enabled U15A so that the arrival of an End Word pulse (J1-14) would again generate a Load and Dump pulse. The two output pulses will continue indefinitely until a reset to U14A is generated as described earlier.

## 2-23. RF Mixer/Amplifier 1A1A7 (fig. 6-10).

*a.* The RF Mixer/Amplifier module contains one gain control attenuator, one balanced mixer, and two RF amplifiers.

*b.* The local oscillator frequency (LO) from the Loop Filter/VCO module is injected into a 50-ohm termination *pi* pad (R1-R3) at J2. The two *pi* pads (R1-R3) and (R4-R6) provide termination and signal attenuation to the LO frequency (approximately 139 MHz to 154 MHz). The signal is coupled through C9 to gain control operational amplifier U1. A voltage divider, R33-R35, allows the gain of U1 to be varied by changing the setting of R34. This bias voltage is monitored at TP2. Capacitors C8 and C10-C13 are bypass capacitors; L5 and R25 are for decoupling. The output of U1 drives the voltage tuned tank, consisting of T1, C15, C16, and VR1. As the tuning voltage (J1-3) is increased, the back-bias on varactor diode VR1 increases causing its capacitance to decrease. This tunes the tank to a higher resonant frequency. Capacitor C15 provides a manual tracking adjustment to the tank circuit. Resistor R14 is a current limiting resistor and C22 is for decoupling.

*c.* The balanced mixer U2 has two input signals, the LO frequency coupled by T1 and the IF frequency (21.4 MHz) from the VCXO module. The IF frequency from VCXO at J3 passes through the 10 db impedance matching pad (R7-R9) and is coupled through T2 to one input of the mixer U2. Transformer T2 and C44 form a tank with its resonant frequency tuned to 21.4 MHz. The center tap of this transformer is biased above ground by the voltage divider R12 and R13. Resistors R10 and R11, with temperature compensation diode CR2, form a voltage divider to bias the LO frequency input to U2. Mixer U2 then outputs to T3 with the mixed LO and IF frequencies. Capacitors C20, C21, and C18 are bypass capacitors; L6 is used for decoupling.

*d.* The secondary of T3 with C24, C27 and VR3 form a voltage tuned tank whose resonance is tuned to the product of the sum of the LO and IF frequencies (approximately 160 MHz to 175 MHz). This frequency is known as the RF frequency. Tuning voltage is applied through current limiting resistor R16 to varactor diode VR3 permitting the tank circuit to track properly through the nine tuning steps. Capacitor C24 allows this tank circuit to be correctly tracked. The two RF amplifiers are identical, so only one is described here. The RF frequency from the tank circuit is applied to gate 1 pin 3 of Q1. Gate 2 pin 2 of Q1 is biased through limiting resistor R17 by the front panel LEVEL SET control R3. The B+ voltage is supplied to this control through R28. The variable output voltage passes through the decoupling network L1 and C3 back to gate 2 of Q2. This change of bias modifies the gain of the amplifier with the bias for gate 1 being derived from the voltage divider R29 and R30. Capacitors C1, C30, C26, C2 and C33 are bypass capacitors. Source bias for Q1 comes from voltage divider R18 and R19. The output of Q1 pin 1 drives the input to T4 which is part of a voltage tuned tank; T4, C32, C34 and VR5. This tank circuit operates the same as those previously described.

*e.* The output of the second RF amplifier (Q2) is coupled through T5 into 50-ohm *pi* pad (R37-R39), the output at J4 then going to the Detector-Output module.

*f.* The tuning voltage applied to each of the voltage tuned tanks is decoupled between stages by networks L7/C28, L9/C35, L12/C38. The +10 vdc line (J1-1) uses C25 and C39 for both low and high frequency filtering.

## 2-24. Mode Control II 1A1A8 (fig. 6-11).

*a.* Mode Control II module will generate the message recycle time delay, insert parity, form the Transmit Gate signal, and produce a sync pulse. Common to these functions is the Reset signal at J1-20 which is a positive going pulse originating from Mode Control I. This pulse is applied to the system at mode change, power application, or end-of-cycle.

*b.* Parity insertion flip-flops, U3A and U3B, receive this reset signal through U4A and invert-

er U4B. This reset is generated when the end parity check pulse at J1–7 is present. When U3A is reset, U3A–2 is a logic one, blocking clock pulses to U3B; U3B–12 is also logic one which prevents U6A from passing any information presented to U6A–1. When the start parity check pulse (J1–6) from the Word Length Generator (1A1A9) clocks U3A–3 the Q output will go to logic zero, enabling U4C to pass the negative-going signal from U4D–11. Gate U4D is an inverter for the positive signal called Parity Clock (J1–2) fro the Shift Register. The positive pulse at U3B–11 will now clock U3B–12 to logic zero, enabling gate U6A. At the start of the 12th bit in the Shift Register a signal, parity insertion (J1–8) is felt on U5D–12. This positive pulse is inverted by U5D and NOR'd by U6A producing a positive-going signal at U6D–12. The negative-going pulse from U6D–11 is NOR'd with the signal gated clock (J1–27) from the Word Length Generator and forms a positive pulse at J1–4 (parity gate to the shift register) At the end of the 18th shift of the shift register, the signal end parity check (J1–7) will cause a reset to the parity flip-flops, U3A and U3B, which will remove the parity gate signal (J1–4, TP2). The gated clock signal (J1–27) may be generated from either fast or slow clocks, so the parity gate pulse may be either 3.3 msec or 833 $\mu$s wide.

*c.* A message recycle time delay is needed to prevent command overlap, eliminate effects of switch bounce and provide adequate reception time by the Radio Frequency Monitor Set AN/USQ–46A. The reset pulse at J1–20 will drive U7C–10 to logic zero, U7B–4 to logic one, and cause the reset of U1A and U10. When U1A is reset pin 2 is a logic one, blocking clocks to U10. The clock pulse to U1A–3 may be generated from several inputs. If either the SEQ–M mode (logic one at J1–13) or the REP–M mode is selected, while not a message type 3 (J1–22) U2A–3 will be a logic zero. This will permit the negative-going pulse $\overline{\text{End Word}}$ (J1–23) to be gated through U2D–11 to pulse high. NOR'd, along with this signal, is the positve pulse Dump from Mode Control I (J1–14). Either of these two signals will cause U2C–10 to pulse low and this pulse will be inverted by U2B to clock U1A. The Q output of U1A, pin 2, will then go to logic zero enabling U6C to pass the signal called Slow (J1–21, 75 Hz square wave). At the negative-going edge of the clock pulse on U10–1, the binary counter U10 will advance one count. The four gates U13A, U13B, U13C and U13D are used to select two count outputs, 40 and 80 counts. Gate U12A will NOR the count of 80 with the auto/manual select line, while U12C will NOR the count of 40 with the auto/manual select line. To determine which count is to be used, examine the inputs at J1–11 and J1–12. If either SEQ–A (J1–12) or REP–A (J1–11) is logic one, we are in the automatic mode. A logic one at the input to U8D will cause U12A–5 to be logic zero and, because of U12B's inversion, U12C–12 to be logic one. Gate U12A is now enabled (count 80) in the auto mode; conversely, in the manual mode U12C (count 40) would be selected. Since the clock rate is 75 Hz, a count of 40 is equal to 530 msec while a count of 80 equals 1 06 second. The positive-going pulse at one of the inputs to U8C will become a negative pulse to the input of inverter U8B. The positive pulse from U8B–4 will latch flip-flops U11A and U11D with U11A–3 low. The flip-flop will remain in this state until the next positive edge of $\overline{2 \times \text{Fast}}$ at J1–18 causes it to reset. This will permit a negative pulse at TP1 of controlled length without regard to the duration of the input pulse. This signal at TP1 is inverted by U7D and a positive pulse is present at U7C. This pulse, through U8B, causes the counter flip-flops U1A and U10 to be reset to their original condition. A delayed reset pulse has been generated whose delay is variable in accordance with the mode selected. In the automatic mode, U8A will be logic zero which allows the negative-going delayed reset pulse at U8A–1 to be gated through. This positive pulse at U11C–9 drives U11C–10 to logic zero and after the pulse is inverted by U11B the positive pulse now clocks both U15B and U15A. Flip-flops U15A and U15B had been reset prior to this pulse by the common reset from J1–20. Gates U9A and U9D have their output pulse low and inverters U9B and U9C would output positive pulses to U15A and U15B respectively. When U15B–11 was clocked by the delayed reset pulse, the Q output of of pin 12 goes to logic zero, enabling U14B to pass the signal Slow (J1–21). When U14B–6 went to logic zero the output U14B–4 went to logic one, causing flip-flop U14A and U14D to latch with U14A–3 low. The flip-flop U14A and U14D will remain in this state until the next positive transition of $\overline{2 \times \text{Fast}}$ (J1–18) which will reset it. This makes a negative going pulse 1.67 msec wide at U14C which is inverted and applied to U9D–12. This will, through U9D and U9C, reset U15B. The output of U14C is utilized as the signal Dump Register to the Word Length Generator. Flip-flop U15 has been preset by the com-

mon reset from J1–20 and can be reset by the end word signal at J1–24. Either of the positive reset pulses causes U9A–3 to pulse low and U9B to pulse high, thereby resetting data gate U15 and producing the signal Data Gate Reset (J1–28) to the shift register. When U15A is clocked, the Q output at pin 1 goes to logic one, remaining in this state until a reset is generated by the End Word signal (J1-24). The output of U15A is called TC (transmit) Gate to Mode Control III. This signal, as well as Dump Register (J1–17), occur 1.06 second after activation of the START button when in the automatic mode.

*d.* The operation of the previously described circuits is similar in the manual mode, however some differences may be noted. Assume that the mode has just been switched from REP–A to REP–M. This generates the common Reset signal at J1–20. Flip-flop U1A will have pin 2 at logic one causing U7A–3 to be logic zero. At this time, Transmit Inhibit from the Word Length Generator at J1–26 would be logic zero making U5A–3 logic one and U5B–4 logic zero. This signal is called Manual Mode Inhibit to Mode Control I from J1–16. In the high logic state the manual mode is inhibited and actuations of the START button have no effect. With Manual Mode Inhibit (J1–16) in the low state, the START button may be activated which simultaneously generates Dump M (J1–15) and Dump (J1–14), both from Mode Control I. Dump M (J1–15) is a positive pulse applied to U11C–8 which, through U11B, clocks U15A and U15B. This, as described previously, forms both a TX Gate (J1–10) and a Dump Register (J1–17) signal. The signal Dump (J1–14), through U2C and U2B, clocks U1A forcing pin 2 to go to logic zero. This logic zero is applied to U7A–2, as is the logic zero from U2A–3 (when in the manual mode). Gate U7A–3 goes to logic one, U5A–3 goes to logic zero, and U5B–4 goes to logic one causing a Manual Mode Inhibit (J1–16) signal. The next activation of the START switch will be inhibited until the recycle delay generator U10 has reached a count of 40 (selected by U12–C when in manual mode) which is a time delay of 530 nsec. We may now state; that when in a manual mode, which is not a type 3 message, if a reset has been generated at J1–20, activation of the start button will produce an immediate transmit signal; subsequent activations must wait for the 530 nsec delay to elapse.

*e.* The output of U15A–1, TX Gate, is coupled through C5 to the base of Q1. Transistor Q1 is an emitter follower with the signal called Sync (J1–29) being routed to the Front Panel Assembly. This signal is used to SYNC external test equipment at the start of the transmit gate. Diode CR1 shunts the negative going spikes to ground to prevent damage to Q1.

*f.* Flip-flop U1B is a delay device for the $\overline{\text{Load}}$ signal from Mode Control I at J1–25. The $\overline{\text{Load}}$ pulse is a negative going pulse which will clock U1B on the rising, or trailing edge of the signal. The next positive going edge of $\overline{2 \times \text{slow}}$ (150 Hz) at J1–19 will reset U1B and restore it for the next $\overline{\text{Load}}$ pulse. The output of U1B–13 is a positive-going pulse at J1–5, Load Delay to the Shift Register while U1B–12 is a negative pulse called $\overline{\text{Load Delay}}$ (J1–3), also going to the Shift Register.

## 2-25. Word Length Generator 1A1A9 (fig. 6-12).

*a.* The Word Length Generator contains a synchronizing circuit whose purpose is to produce a pulse at J1–17 ($\overline{\text{Act Syn}}$), which is synchronous to all system clocks. This circuit consists of U2D, U9B, U9C and U12A through U12D. Operation of the synchronizer is the same as the circuit described in paragraph 2–22*b*. Signals from the front panel START button (S11) are applied to J1–26 ($\overline{\text{Activate Switch}}$) and J1–33 (Activate Switch) which become inputs to the flip-flop U2B and U2C. This flip-flop eliminates the effects of switch bounce. Normal condition on the START switch (S11) applies a logic zero to U2C–8 and a logic one to U2B–5 and since the START switch (S11) can supply only a logic one signal, R4 and R6 are pulldown resistors, when a line is open from the switch S11. When the START button (S11) is pressed, U2C–8 goes to logic one and U2B–5 goes to logic zero causing the flip-flop to latch U2B–4 at a logic one. This condition remains until the START button is released. The logic one at U2B–4 becomes the input signal to the synchronizer which produces a negative-going 6.67 msec pulse at U18B–12. Circuit U18B receives three clock inputs: $\overline{2 \times \text{Fast}}$ (J1–11), $2 \times \text{Slow}$ (J1–31), and $\overline{\text{Fast}}$ (J1–32). To reduce the width of the pulse at U18B–12, it is NOR'd with clocks to produce an 833 $\mu$sec wide positive pulse at output U18B–13 (fig. 2–24). This pulse is inverted by U4D to become the $\overline{\text{Act Syn}}$ pulse at J1–17 (to Mode Control I).

*b.* The reset pulse generator consists of compo-

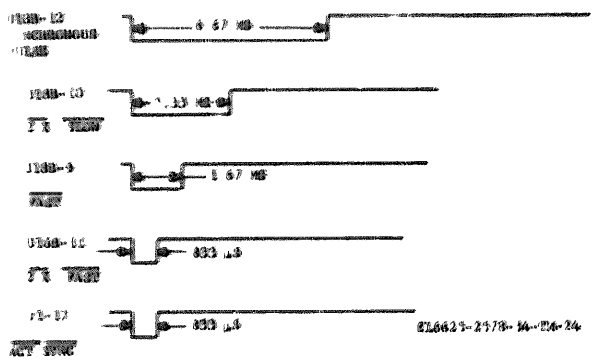


Figure 2-24. Clock timing diagram.

nents VR1, R8, C2 and U1D. When power is first applied to the system both U1D–12 and U1D–13 are logic zero, causing the output to go to logic one. Varactor VR1 reduces the value of the voltage applied to RC network R8 and C2 to set the charge time of C2 to about 50 msec. When the voltage at C2 reaches the gate voltage of U1D–12 the output will go to logic zero, removing the reset signal called PWR ON RESET (J1–19).

*c.* The word length detector will count and decode system clocks according to the message type and keying rate selected, and generate Parity Timing pulses and an End Word pulse. Keying rate information, in the form of signals called FSK S (J1–24) and FSK F (J1–25), are NOR'd along with two system clocks Slow (J1–30) and Fast (J1–35). When the selected keying rate gate signal goes to logic zero, its associated clock is gated through either U1A or U1B and NOR'd by 11C, whose output is a continuous 75-Hz or 300-Hz clock train. When a positive going Dump Register pulse (J1–10) arrives from Mode Control II, flip-flop U3A will be clocked. Chip U3A had previously been reset by the End of Word pulse, the next clock will cause U3A–1 to go to logic one and U3A–2 to go to logic zero. Gate U3A–1 becomes the X-Mit Inhibit signal (J1–18) to Mode Control II while U3A–2, now at logic zero, enables U4C to pass the clock train on pin 9 of U4C. The output of U4C–10 is the signal Gated Clock (J1–4) and becomes inverted by U2A which clocks U10. Component U10 had been reset prior to this time by Dump Register signal (J1–10) which initiated the Gated Clock sequence. See figure 2–25 for a timing diagram of the message length decoder. Component U10 is a 7-stage binary counter whose first five outputs are presented in their true and not-true states to the decoder gates of U13A, U13B, U14A and U14B. Gates U11A through U11D and U6C invert the true signals to not-true signals used by the decoder gates. Decoding provided by U-13A provides a positive going pulse, one clock wide, during the 12th clock which is start parity check (J1–6) to Mode Control II. The output of U13B is inverted by U15A and NOR'd by U16D $2^5$ to form a positive pulse during the 17th bit, one clock wide, called Insert Parity (J1–8) to Mode Control II. The signal from U14A is inverted by U15B and NOR'd with $2^6$ by U17A to form the signal End Parity Check (J1–7) to Mode Control II, which begins with the 19th bit and ends with the 20th bit. It is noted, that parity is checked only on the message bits of an 18 bit word and that additional bits accompanying a 24-bit word are not checked for parity.

*d.* Message types 2A and 2B are 24 bits long and message types 1 and 3 are 18 bits long. If either a 2A or 3B message is selected, one of the inputs to U7A will go to logic one causing U7A–3 to go to logic zero. This logic zero is inverted by U7D placing U17C–9 at logic one and blocking the decode 18 line. The logic zero from U7A–3 goes to U9A which is then enabled; U9A NOR's the inverted information from U14-B–13 along with $2^5$ from U6C–10 to provide a positive going pulse at the end of the 24th clock. This pulse is inverted by U17D (U17D–12 is now logic zero) and again inverted by U16A to generate a positive pulse to the end word flip-flop U16B and U16C. This positive input at U16B–5 latches the flip-flop with U16B–4 to logic zero; this condition remaining until a reset is provided by 2 x Fast at U16C–8. A negative pulse has been generated at J1–15 called End Word and an inverted pulse (inverted by U16D) called end word at J1–16. The signal End Word (TP2) returns to gates U5A and U4A; these gates, through inverters U5B and U4B, cause the reset of U10 and U3A respectively. The counter/decoder system has been restored to the conditions existing before the Dump Register signal (J1–10).

*e.* Message type 3 is an 18 bit word followed by a 20.5-sec audio burst if in the REP M Mode. If a message type 3 is selected, J1–21 and J1–22 will both be logic zero causing U7A–3 to go to logic one, selecting the gating necessary to provide an End Word pulse at the end of the 18th clock. At the same time J1–23 (3) would be logic

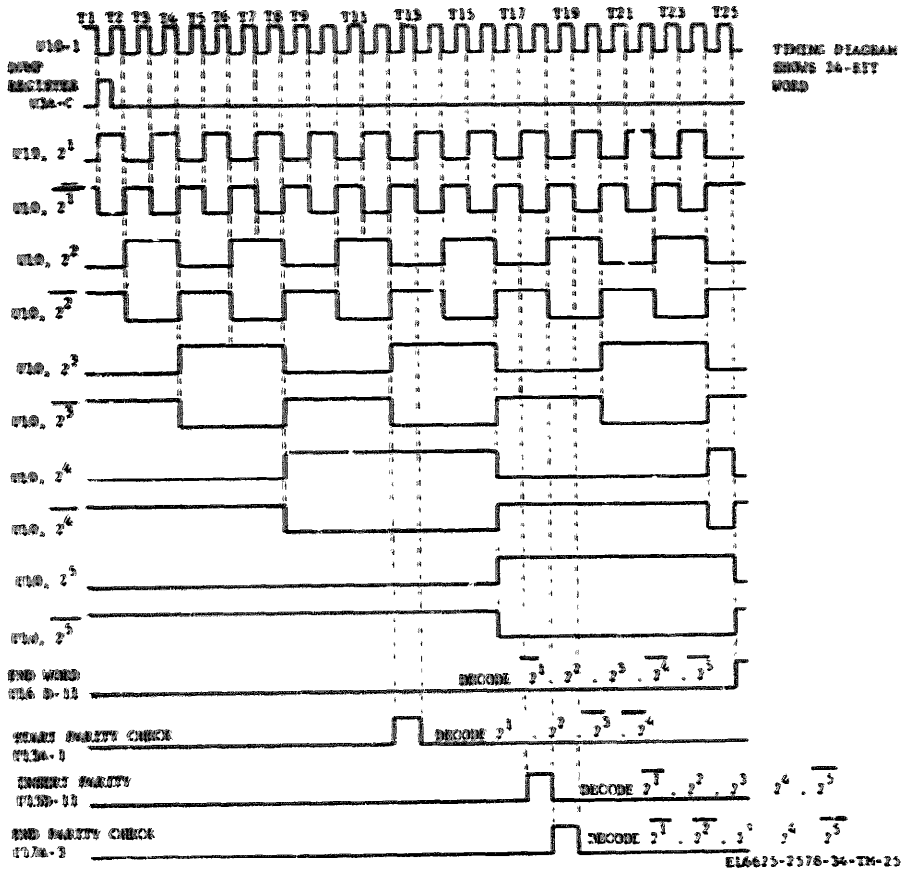



Figure 2-25. 24-bit word timing diagram.

one causing U7B–4 to go to logic zero and enabling U5C–11. REP M, if selected, will place a logic zero on J1–34 enabling U5C–12 and U7-C–9. U7C–10 would be logic zero, this being the signal 3 REP M at J14 (to Mode Control II). With both pins 11 and 12 at logic zero, U5C now passes the negative-going pulse, End Word (J1–15), to clock U3B. Flip-flop U3B has been reset prior to this time by the signal Audio Gate Reset (J1–28) from Encoder 1 so the clock pulse will cause U3B–13 to go to logic one and U3B–12 to go to logic zero. When the next Audio Gate Reset signal arrives, 20.5 sec later, U3B will again be reset and the pulses Audio Gate (J1–26) and Audio Gate (J1–29) will have been generated. Components U6A and U5B are no longer functional in this mode due to design modifications.

2-26. Reference Generator 1A1A10 (fig. 6-13).

*a.* The Reference Generator receives a frequency of 3.75 MHz from the TCXO at J2. The 3.75 MHz clocks U1 on each negative-going slope and, with all J and K inputs wired to B+, U1 then divides its input by 2. The Q output (1.875 MHz) of U1 at pin 11 is coupled through C6 to the emitter of transistor Q1. Transistor Q1 is a blocking oscillator consisting of components Q1, T1, R5, R8, C13 and C5. As Q1 is turned on by the input signal, current is drawn through the A/B coils of T1 which induce a positive feedback signal into the C/D coils. This signal is coupled through C5 to the base of Q1, driving it quickly into saturation. Capacitors C13 and C22 are bypass capacitors, CR1 and CR2 provide transient protection. The output of the oscillator (TP4) is a very narrow pulse, rich in harmonic frequencies (spectrum). This output is injected into the 50-ohm impedance matching *pi* pad made up of R3, R6 and R25, with R6 selected so that all spurs fall between the −30 dbm and −35 dbm levels. The spectrum output then connects to the Synthesizer/Mixer.

*b.* The $\overline{Q}$ output of U1 at pin 12 (1.875 MHz)

is coupled through C9 and C10 to the bases of Q2 and Q3 respectively. Resistors R9, R10 and R11 complete the circuit which is connected as a totem pole level translator. When the output of U1-12 goes to logic one (+5V) Q3 is pulsed on, placing TP3 at ground; when U1-12 goes to logic zero Q2 will be pulsed on, causing TP3 to go high (7.2V). The level translator satisfies the input requirements of U2, U3 and U4A. Components U2, U3 and U4A are connected as a Johnson decade counter; this configuration requires ten clock inputs before the counter returns to its original or starting state. With each positive transition of the clock line the level present on the D input will be transferred to its associated Q output. When U2A-1 and U2B-12 go to logic one, the anodes of CR3 and CR4 will be pulled high through R17, causing U3 and U4A to be reset. When power is first applied or interrupted, the decade counter may be in any logic state, but during the first cycle, a reset will be generated to introduce the proper logic levels to the system. Capacitor C14 is a speedup capacitor; diodes CR5 and CR6 provide protection against negative spikes. The output of U4A at pin 2 (divide by 10) drives a second divide by 10 stage (U4B, U5 and U6). This stage operates in the same manner as the first divide by 10 counter with the sum of the two division factors now equaling 100. The input of 1.875 MHz (TP3) has been divided by 100 to become 1.875 kHz Reference Output.

*c.* The 3.75 MHz signal (monitored at TP2) is coupled into a double tuned bandpass filter made up of components C3, C4, C29, C30, C32, C33, L2 and L3. The first and second poles are coupled by C11, with the output being tuned to the 4th harmonic of the input (15 MHz). The 15 MHz signal is coupled through C15 into a 6 times multiplier consisting of components Q4, Q5, T2, the secondary of T3, R12-R16, R18, R24, R26 and C34. Capacitors C17-C21 are bypass capacitors. Resistor R12 and R13 provide the bias for Q4, while R15 and R16 do the same for Q5. The signal developed by Q4 is transformer coupled to the base of Q5, Q5's output is coupled through T3 into a 2-pole filter which will select the 90-MHz frequency for an output. The first pole filter consists of T3's primary and C2; the second pole consists of L7 and C1. Capacitor C24 couples the 2 poles while the output (monitored at TP1) is coupled through C26 to a 50-ohm impedance matching Tee pad, R21-R23. The 90-MHz output routes to the Synthesizer/Mixer from J3.

*d.* Chokes L1, L4-L6, and L8 are used to decouple the B+ lines in each of the various circuits just described. Capacitors C25 and C28 are filters for the 5 vdc and 7.2 vdc lines respectively.

## 2-27. Mode Control III 1A1A11 (fig. 6-14).

*a.* The Mode Control III module receives a 600-Hz clock (2 x Fast) at J1-2, which originated in the Encoder II module. When power is first applied, a positive-going pulse is felt at J1-5 which resets U3 and U2B to the proper conditions needed to maintain correct clock relationship from these flip-flops. The 600-Hz signal is the clock for flip-flop U3A which divides by 2, and whose Q and $\overline{Q}$ outputs are Fast (J1-4, 300 Hz) and $\overline{\text{Fast}}$ (J1-8, $\overline{300\ \text{Hz}}$) respectively. The Fast clock also clocks U3B whose Q output is called $\overline{2 \times \text{Slow}}$ (J1-7, $\overline{150\ \text{Hz}}$). The Q output of U3B pin 13, clocks another flip-flop, U2B, which divides the frequency by two to produce Slow (75 Hz) at J1-3 and $\overline{\text{Slow}}$ ($\overline{75\ \text{Hz}}$) at J1-6. These clocks are used throughout the system to maintain correct time sequences.

*b.* The clock 2 x Fast (J1-2) is inverted by U1D to become a clock for flip-flop U2A. The signal Burst Generator Gate is present at J1-13 as a positive going signal from the Encoder II module. When this signal is logic zero (Burst Generator Gate not present) U1C inverts this logic zero and presents a logic one level to the reset of U2A, pin 4, and this causes U2A-1 to be logic zero. When the Burst Generator Gate goes to logic one, the reset (U2A-4) is removed and the next negative transition of 2 x Fast (J1-2) is removed and the next negative transition of 2 x Fast (J1-2) is inverted by U1D to clock this data through U2A-1. The output at J1-14 is the Burst Generator Gate delay to Mode Control I. When the Burst Generator Gate (J1-13) goes to logic zero, an immediate reset is generated to U2A returning U2A-1 to its logic zero state.

*c.* For the VCXO (1A1A1) to produce an IF frequency, the 21.4-MHz oscillator must be turned on by the VCXO Gate (J1-10). This positive signal may be generated by a number of conditions determined by the front panel control settings. If any of the following signals are logic one, a VCXO Gate will be generated: EXT MODE (J1-26 through CR6), CAL (J1-24 through CR3), or AUDIO GATE (J1-11 through

CR4). If the negative-going Date Gate signal from the Shift Register (1A1A15) is present at J1–20, U7D inverts this information and applies it to U6A–5. Flip-flop U6A had been reset prior to this time by the positive state of the Data Gate signal and consequently, U6A–2 was at a logic one level. On the next positive transition of the signal Fast at U6A–3, the Data Gate signal is clocked through to become a negative level at U4A–1. If the FSK–F key [illegible] is not selected (logic zero at J1–22), output of U4A–3 will go to logic one causing a VCXO Gate signal (through CR1) at J1–[illegible] soon as the signal Data Gate (J1–20) goes to logic one, the VCXO Gate is removed. Had the FSK–F signal been selected, U4A–3 would have been a logic zero and U4D–11 would have been logic zero. The positive going TX Gate signal (J1–12) will be clocked through U6B by the next concurrence of logic zero signals at U7C–8 (Fast) and U7C–9 (2 x Slow). This clock pulse is delayed from the clock at U6A–C by 5 msec, producing a delayed negative-going TX Gate at U4-B–6 which is enabled in the FSK–F position. The output of U4B pin 4, will go to logic one causing a VCXO Gate (J1–10) through diode CR2. When TX Gate (J1–12) goes to logic zero, the VCXO Gate will return to its low state.

*d.* If REP–A (J1–17), REP–M (J1–18), SEQ–A (J1–15) or SEQ–M (J1–16) is selected, a logic one level will be present on the anode of its respective diode which causes U5B–13 to go to logic one. U5B–10 then goes to logic zero and enables U7A to pass the Data Gate signal on pin 2 to J1–28 (VCXO–C). This signal, when logic zero, permits data to be gated on by the VCXO module. If either INT MOD (J1–25), or EXT MOD (J1–25), or EXT MOD is selected, a logic one will be seen through either CR9 or CR10 at U5B–11. U5B will enable U7A to pass the signal called VCXO–C at J1–28. If a logic one is present at J1–21, a Message Type 4 has been selected and both U5A–5 and U5B–12 will be logic zero. Gate U5B will gate the VCXO–C signal to (J1–28) while U5A will, if CAL is selected (J1–24 logic one), pass the 75-Hz signal on U5A–3. This 75 Hz, through CR11, will become the modulation signal to the VCXO for calibration of the front panel DEVIATION METER, M1. If the CAL MODE is not selected, U5A–4 will be logic one, U5A–6 will be logic zero, and the modulation signal will originate from the Shift Register. The Manchester coded data is called Data Out at J1–23 and is presented to the anode of CR12 to become the signal VCXO–B (data modulation, J1–27).

*e.* When the INT MOD position is selected (J1–25 high) or an Audio Gate is present (J1–11 high), CR7 and CR8 respectively will pull (J1–29) 1-kHz Gate to a logic one. This signal goes to the VCXO and turns on the internal 1-kHz oscillator.

## 2-28. Encoder I 1A1A12 (fig. 6-15).

*a.* Encoder I receives a negative-going signal at J1–18 from the Word Length Generator at the beginning of the Audio Gate. The Audio Gate signal at U1A–1 enables the 75-Hz clock (Slow) on U1A–2 to be gated through to the output at pin 3. Both U3 and U5 are 7-stage binary counters that had been reset prior to the introduction of the Audio Gate signal. The reset cycle follows later in this discussion. It requires 128 clock inputs to U3–1 to generate one output pulse at U3–4, this being inverted by U1B to become the clock to U5. When U1D–13 and U1C–8 receive high levels at the count of 12 from U5, both U1D–11 and U1C–10 will go to logic zero. This point in time corresponds to 1536 clock pulses (127 x 12) or 20.4 sec after the Audio Gate signal was received at J1–18. With both inputs to U10A a logic zero U10A–3 goes to logic one and latches the flip-flop U10B/U10C. The output at U10B–4 will go to logic zero until this flip-flop is reset by the next positive transition of 2 x Fast (J1–14) at U10C–9. The negative pulse at U10D–12 is inverted by U4A and reinverted by U4C to become the reset to U3 and U5. An output pulse of 20.4 sec has been generated at J1–17 which routes to the Word Length Generator. The reset of U3 and U5 could also have been accomplished by a positive-going reset signal at J1–15. This signal occurs when the START button (S11) is pressed, or when power is applied at the end of cycle. A mode change will also cause a reset to be generated through U4A and U4C.

*b.* If either the SEQ–A (J1–12) or the SEQ–M (J1–13) modes are selected, one of the inputs to U2A will be logic one causing U2A–3 to a logic zero. This logic zero is inverted three times by U2B, U2D to U6D successively to become a logic one at U7–6 and J1–20, Set Carry to Encoder II. A logic one at U7–6 has no effect on the operation of U7. When the START but-

ton (S11) is pressed, the Reset pulse at J1–15 is inverted by U4D to become a negative pulse at U2C–9 whose other input, pin 8, is a logic zero in either SEQ MODE. This causes a positive pulse at U2C–10, which is inverted to become a reset to U7–9. This pulse is called Reset Carry at J1–19 which is relayed to Encoder II. This negative-going pulse at U7–9 causes U7–3 to go to logic one while U8, U11, U13 and U15 have all their Q outputs reset to logic zero by the signal at J1–15. Each time a positive going End Word pulse is felt at J1–32, all flip-flops (U7, U8, U11, U13, and U15) will have the information on their D inputs (J input for U7) clocked through to their respective Q outputs. Prior to the first End Word pulse, U7's Q output was the only one at logic one, so when all the flip-flops are clocked this logic one will advance one stage, to U8A. U7–3 is at logic zero because of its input from U15B–13 during the first clock. On the eighth clock pulse, U15B–12 will go to logic zero and on the ninth clock pulse, will go to logic one. After nine clock pulses a Seq Count Carry signal at J1–21 is generated to the Encoder II module, and the Shift Register U7, U8, U11, U13 and U15 is returned to the starting logic levels. If either of the repetitive modes have been selected, U2A–3 would be at logic one, U2C–10 would be logic zero, and U6C–10 would be logic one, not placing a reset signal on U7–9. The logic one at U2A–3 would be inverted by U2B, enabling the negative-going reset pulse from U4D–11 to be gated through U2D After being inverted, the positive pulse applied to U7–6 will place U7–3 at logic zero; therefore, the End Word pulses at J1–32 will have no data to clock through the shift register and all Q outputs will remain logic zero.

*c.* The data Select gates consist of U6A, U6B, U9, U12, U14 and U16. Since the operation of all these gates is identical, U6A and U6B will be used as examples. If the repetitive mode is selected, the Q output of U7, pin 3, will be logic zero enabling U6A to pass the signal on pin 1. This signal will come from J1–23 which routes to the PROGRAM SELECT switch S5 and may provide a logic one or zero in the repetitive mode. If U6A–1 is at logic one, U6A–3 will be logic zero causing U6B–4 to go to logic one; conversely, if U6A–1 is at logic zero, U6B–4 will be logic zero. This signal is called Decode 9–1 and routes to the Encoding Matrix as units information. If the SEQ MODE had been selected, the logic one on the common line of the PROGRAM SELECT switch (S5) would have been removed and pulldown resistor R1 would have placed a logic zero on U6A–1. The information, in this case, would come from the Q output of U7 pin 3.

2-29. Encoding Matrix 1A1A13 (fig. 6-16).

*a.* The Encoding Matrix receives units information (Decode 9–1 to 9–9) from Encoder I and tens information (Decode 7–0 to 7–7) from Encoder II. This information, after passing through the encoding matrices, exit as coded and binary data to the Shift register. The PROGRAM select switches, through Encoders I and II, pass information which is encoded by the Encoding Matrix to a format that represents, in the Shift Register, the actual transmitted word. Chips U1 through U16 are diode matrixes that have had some of their internal fusible links intentionally blown to provide each unit with separate coding structures. These matrices, along with discrete diodes CR1 through CR64 and resistors R1 through R64, form the encoding system.

*b.* The matrix can best be discussed by the use of an example. Consider the case where the mode is repetitive and the PROGRAM select switches are in a position to cause Decode 9–9 (J1–23) and Decode 7–0 (J1–22) to be logic one; all other signals are logic zero. Decode 9–9 places a logic one on the register string R1 through R6 while Decode 7–0 places a logic one on the cathodes of CR1, CR17, CR25, CR33, CR41, CR49 and CR57. For a line to go to logic one, it is required that both its cathode and resistor/anode line be a logic one; in this case the anode line to CR1 is the only one that qualifies. This places a logic one on pin 14 of both diode matrices U1 and U2. Refer to the diagram which shows the internal coding of both these matrices (fig. 6–16②). When pin 14 of U1 goes to logic one, the diodes associated with lines 3, 11, 4, 5 and 6 pull these lines to a logic one, while all other lines are logic zero. These pins are routed to the data outputs called $2^1$, $2^2$, $2^3$, $2^4$ and $2^8$ coded. Pin 14 of U2 going to logic one pulls lines 11 and 6 high which are the outputs $2^1$ and $2^4$ binary, respectively. All other input codes may be followed through the Encoding Matrix in the same manner.

2-30. Encoder II 1A1A14 (fig. 6-17).

*a.* Encoder II module contains the same type of shift registers and data gates as Encoder I (para 2–28*b*). The shift registers U2, U6A, U8, U13 and U16 will function as the source of sequential

coding for the tens information which is fed to the data selector gates. The Set Carry (J1-20) and the Reset Carry pulses (J1-19) are the same pulses applied to Encoder I shift registers and perform the same function. Once the initial logic one is obtained at U2-3, the data shifting occurs with each SEQ CT CARRY (J1-21) that is generated when the encoder I shift registers advance through one complete count cycle. The data gates receive, either sequential coding information or, if in the repetitive mode, tens program select information from the front panel switches. This data is routed to the tens inputs to the Encoding Matrix.

*b.* A frequency of 13.75 kHz (J1-23) is the clock to binary counter U1. Signals $2^1$ through $2^4$ are inverted by U5 and the four outputs are NOR'd by U7B. The output of U7B, approximately a 5-$\mu$sec pulse, is inverted by U4D and NOR'd with the inverted $2^4$ output of U1 to produce a positive pulse at U4B-4. This pulse, or the positive PWR ON RESET pulse of J1-15, will cause U12D-11 to pulse negative, this is inverted by U12C and becomes a positive reset pulse at U1-3. This resets counter U1 as near as possible to the desired 600 Hz output at U1-6 (monitored at TP2).

*c.* When Encoder I and Encoder II module shift registers reach the point where 64 codes have been sequenced, both U10B-6 (J1-22) and U10B-5 (from U16B-12) will be a logic zero causing U10B-4 to pulse to logic one. This logic one will latch flip-flop U10A/U10A with U10A-3 to logic zero; this output is inverted by U10C to become a positive pulse (monitored at TP1) called End of Cycle and routed to Mode Control I. Flip-flop U10A/U10D, is reset at U10D-13, by the next positive-going edge of the 600 Hz clock) $\overline{2 \times \text{Fast}}$ at J1-12).

*d.* A positive pulse is present at J1-16 (Burst Gen Reset) whenever the START button (S11) is pressed, power is applied, end of cycle, or MODE switch (S7) is changed. This pulse resets both U15B and U18. With U15B-13 now reset to logic zero, 600 Hz clocks will be gated through U12A to clock binary counter U18 and become the signal Burst Gen Clock to the Shift Register module (monitored at TP4). After 32 clocks, U18-5 goes to logic one and causes U15B to be clocked which then makes U15B-13 a logic one and stops the clocks at U12A-3. The output at U15B-12 is a positive pulse occurring when the reset (U15B-10) is present and lasting for a duration of 32 600-Hz clocks (53.4 ms). This signal is Burst Gen Gate to Mode Control III.

When the front panel MODE switch (S7) is in SEQ position, the logic level on U9B-5 (J1-22) will be a logic one. This logic one is inverted to become a logic zero at U9C-9 which will enable the positive-going PWR ON RESET (J1-15) pulse to be gated through. This pulse, after being inverted by U9D, is a positive-going reset signal to U15A that will latch U15A-2 at logic one. With U15A-2 a logic one, the output of U12B-4 is held to logic zero (SEQ A Initiate, J1-33). When the START button (S11) is pressed, in the SEQ A mode a positive-going pulse is applied to J1-32 from Mode Control I. This pulse will clock U15A and set Q output at pin 2 to logic zero, enabling the Burst Generator Gate (J1-17) to be passed by U12B. The output at J1-33 then, is the invert of Burst Gen Gate when in SEQ A mode. If SEQ A mode is not selected, J1-34 is logic zero, U9B-4 is a logic one, U9C-10 is a logic zero, U9D-11 is a logic one and U15A is held in the reset condition with its Q output at logic one, holding the SEQ A Initiate (J1-33) a logic zero.

### 2-31. Shift Register 1A1A15 (fig. 6-18).

*a.* Data to be transmitted is assembled in the Shift Register in the correct order by parallel entry of information, and is then serially shifted out. Six-bit coded data from Encoding Matrix is present at J1-8 and J1-10 through J1-14. Six-bit binary information, from the Encoding Matrix, is presented at J1-2 through J1-7. Message type information is on J1-15 and J1-16 with its source being the Word Length Generator. Resistors R1-R12 serve as pulldowns for the output lines from the Encoding Matrix. Gate U2A-5 is tied to +7.2V; this assures that all the cells in the shift register have their Q outputs at logic one at load time, because of this level being shifted through the register with each clock input. When the Load Delayed pulse from Mode Control II module arrives at J1-19, the negative gate permits input gates U1C, U1D, U4, U10 and U14 to pass data to the reset lines of their respective shift register cells. When the input data line at logic zero, the reset to the cell will go to logic one, causing the Q output to go to a logic zero; should the input data line be a logic one, the reset line will remain a logic zero and the Q output will remain in its logic one state. Cell U17B represents the sync bit and

has its Q output a logic one due to the logic one shifted through it from the previous word. The SYNC bit will always be a logic one. Cell U9A is a logic one, representing the 18th or parity bit, and has its output level modified as necessary after the six bits of coded data have been checked for parity. Cell U18A hold the information preceding the actual data word and is not part of the actual word itself. The Load Delayed pulse at J1-23 goes positive at the same time as the Load Delayed pulse goes to a logic zero. The positive Load Delayed pulse goes to a logic zero. The positive Load Delayed pulse places a reset on U3, U6, U8, U11A and U18A causing their Q outputs to go to logic zero.

*b.* After all information has been gated into the shift register cells, J1-21 will receive the signal Gated Clock (either 75 Hz or 300 Hz). This will be NOR'd by U1A with the Burst Generator Clock at J1-17 (600 Hz). The subsequent output of U1A-3 is inverted to become the shift register clock. With each positive going transition of the clock, the data in the shift register is shifted into the Manchester encoder (U15A, U15B and U15C). The output of U15A becomes Parity Clock to Mode Control II and is used by the parity check circuit to determine parity of the 12th through 17th bits. Between the 17th and 18th bits, a signal called Parity Gate (J1-20) is a logic one or logic zero as needed to inject a parity bit into cell U11B, which, with the next clock, becomes the 18th or parity bit out.

*c.* When the first Gated Clock at J1-21 goes positive U18B is clocked, placing U18B-12 a logic zero; this permits Manchester coded data from U15C-10 to be gated by U15D and become Data Out at J1-22. This output data becomes one of the modulation sources to the VCXO. When an End Word pulse is generated from Mode Control II at J1-24, flip-flop U18B is reset. This causes U18B-12 to go to logic one and block U15D from transmitting any data. The Q output of U18B is also the Data Gate Signal at J1-25 which routes to Mode Control III.

*d.* The Q and Q outputs of U18A are used along with the Gated Clock and Gated Clock signals to generate Manchester coded data at U15C-10 (see example of Manchester coding, fig. 2-26). The Manchester coding, received by the AN/USQ-46, provides both signal intelligence and clock information while being a more secure transmission code.

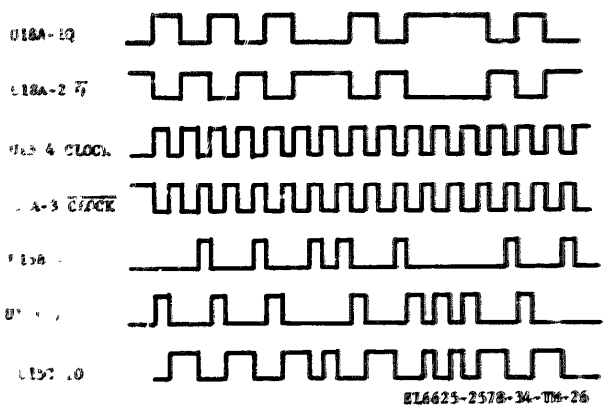



Figure 2-26. Manchester encoded data, example

## 2-32. TCXO 1A1A16

The TCXO (Temperature Compensated Crystal Oscillator) generates an output frequency of 3.75 MHz with a stability of ±1 ppm. The crystal and associated electronics are housed in a hermetically sealed case for stability throughout a temperature range of −65° to +155° F. By removing an access screw in the case, small adjustments may be made to the output frequency. Other than access to the frequency adjustment, the unit is completely sealed and cannot be repaired.

## 2-33. Power Supply/Regulator 1A1A17 (fig. 6-19).

*a.* Zener diode VR1 provides a reference voltage to the base of Q2 through R2; this acts as a constant current source for VR2, VR3 and VR4 under variations in the input voltage.

*b.* Zener diodes VR3 and VR4, in series with CR2, provide the reference voltage to the emitter follower Q3 (3.6 Vdc at E4) and to emitter-follower Q4 (7.2 Vdc at E5). The reference voltage on the base of Q4 may be monitored at TP3.

*c.* Zener diode VR2, in series with CR1, provides the reference voltage to the emitter-follower Q1 which supplies +5 vdc to E2.

*d.* Zener diode VR5, in series with CR3, provides a reference voltage to emitter-followers Q5 and Q6, both of which supply +10 vdc to E6 and E7.

*e.* Diodes CR1, CR2 and CR3 cancel the base-emitter drops of their associated transistors to obtain the proper output voltage levels.

*f.* In the Front Panel Module Assembly (1A), Zener diode VR1 (through constant current diodes IR1 and IR2) provides the tuning voltage reference of 7.08 vdc.

2-34. Front Panel Assembly 1A1A18 (fig. 6-20).

*a.* The front panel meter (M1) works in conjunction with the RF level set control (R3) and the deviation level control (RL) to provide a visual output indication according to the position of the METER switch (S10). Rotation of either R1 or R3 clockwise will increase the meter indication for the selected mode.

*b.* The RF output attenuator will attenuate the output signal in steps of 1 db ranging from 0 db to 121 db (−db to −131 db).

*c.* Fuse F1 is in series with the input powerline and the MODE switch (S7) which controls the power ON/OFF condition. The MODE switch (S7) may also select any of the Repetitive or Manual Modes as well as CAL, INT, or EXT modulation positions. Actuation of the START switch (S11) will regain the selected program sequence.

*d.* Keying rate and deviation is selected by the FSK switch (S8). Four available message types may be selected by the MESSAGE switch (S9).

*e.* The two PROGRAM switches. S5 and S6, select the message to be transmitted when a repetitive mode is used. RF CHANNEL NUMBER switches, S1, S2, S3 and S4 are positioned to one of the 2520 RF channels available.

*f.* Jacks are provided for External Modulation input (J2) RF output (J3), SYNC output (J4) and VIDEO output (J1).

2-35. Power Supply (PP6446A/USQ-46) 2A1 (fig. 6-21).

*a.* Power supply PP6446A/USQ-46 is designed to operate on either 22 to 33 volts dc or 100 to 132 volts ac at 50-60 or 400 Hz and output a regulated and unregulated dc voltage.

*b* In dc operation, 22 to 33 volts input is applied between J1-J and J1-M, J1-A and J1-B are jumpered together. Feedthrough filters FL1-3 and FL-7 provide EMI protection at input connector J1. Ferrite beads Z1-Z5 provide EMI protection at output connector J2. Fuse F2 provides normal circuit protection and is supplemented by a high voltage transient suppression network consisting of L2 and C6. Diode CR2 provides reverse current protection. Components Q1-3, R1, R4, CR6-7, VR1 and C4-5 make up the unregulated dc voltage network. Overvoltage protection for the unregulated supply is provided by VR1, a 33-volt Zener diode. Transistor Q2 is a current amplifier and supplies sufficient base current to Q1 through Q3. The configuration of Q1-3 maintains a single junction voltage drop between the emitter of Q1 and base of Q2. Diodes CR6 and CR7 provide short circuit protection for the unregulated supply. During normal operations, CR6 and CR7 are back biased. Should a short circuit condition occur, they become forward biased and shunt the current to ground. Capacitors C4 and C5 provide filtering to diminish the effect of any ac components. The output of the unregulated supply is routed to the 12 volt regulator circuit and to pin E of output connector J2. The regulated dc circuit is composed of Q4, VR2, CR3-5, CP8, R2-3, and C3. Zener diode VR1 (13 volts) provides both overload protection to the regulated supply and a constant voltage source to transistor Q4. Diodes CR3 and CR8 set a reference pedestal for short circuit protection diodes CR4 and CR5. Short circuit protection is accomplished in the same manner as for the unregulated circuit. Capacitor C3 provides additional filtering to the output The output is routed to pin 13 of connector J2.

*c.* In ac operation, 100 to 132 vac is applied to pins J and L of connector J1. Jumpers are across pins A to K and B to C of J1. Feedthrough filters FL1/FL7 provide EMI protection at the input connector J1, and Ferrite beads Z1/Z5 provide EMI protection at the output connector J2. Fuses F1 and F3 provide normal circuit protection. Transformer T1 steps the 100 to 132 vac input voltage down to approximately 33 vac Full-wave rectifier, bridge network CR1, rectifies this voltage and routes it through a filter network of L1, C1 and C2 to the unregulated dc voltage circuit. See *b* above for description of dc voltage processing.

# CHAPTER 3

# DIRECT SUPPORT MAINTENANCE

## Section I. GENERAL

### 3-1. Purpose.

*a. General.* Information contained in sections I through III of this chapter is designed to aid the repairman in detecting and correcting test set troubles caused by faulty modules. Section IV contains removal and replacement instructions for repair of the test set and section V contains test procedures with performance standards to check the serviceability of repaired equipment. Sections VI and VII contain information required to perform direct support maintenance on the power supply.

*b. Operational Indications.* Module test point waveforms and terminal board voltage and resistance measurements of an operational test set are provided in this section to aid in isolating a trouble. Location of modules, with their test points, and major components are provided in paragraph 3–4. Voltage and resistance measurements are provided in paragraph 3–5 and system test point waveforms are provided in paragraph 3–6. In addition to this troubleshooting data, abnormal indications of a test set are provided in the troubleshooting chart (para 3–9).

### 3-2. Repair Procedures

*a. General.* When equipment has been turned in for repair, first check it for completeness and condition. Check the preventative maintenance forms to find deficiencies that could not be corrected at the organizational maintenance level. Check for equipment tags that may indicate the equipment malfunction.

*b. Inspection.* Make a visual inspection to determine the condition of the equipment when it is turned in for repair. Remove the center housing assembly from the Test Set (para 3–13) and inspect the equipment as follows:

(1) Inspect all accessible components for indication of burning.

(2) Inspect for broken leads or leads with brittle or damaged insulation and corrosion.

(3) Inspect all plugs for proper seating, loose or broken leads, poor solder connections.

(4) Inspect fuse holder for bent contacts, damaged cover, and corrosion.

(5) Check the operation of all switches. They should have positive action and be free of corrosion.

*c. Corrective Action.* Locate malfunctions in accordance with the procedures of sections I through III and remove and replace parts in accordance with the procedures of section IV. Verify the serviceability of repaired equipment in accordance with the procedures of section V.

### 3-3. Troubleshooting Data.

Reference data consisting of component location illustrations, voltage and resistance measurement charts, and module test point waveforms are provided in this section for the Test Set and power supply. In addition, the following troubleshooting data is referenced to aid the repairman in rapidly locating a trouble:

*a. Wiring Diagrams.* The test set wiring diagram (fig. 6–2) shows interconnection between modules, assemblies, and piece parts (controls). The power supply piece parts are hand wired together. Therefore, the power supply schematic diagram serves as a wiring diagram also.

*b. Block Diagram.* The overall functional block diagram (fig. 6–3) covers the functional interrelationship between the radio test set modules, front panel assembly controls, and power supply circuits. Module and system input and output signals are defined and location of module test points are shown in the functional block diagram.

*c. Schematic Diagrams.* Schematic diagrams for each radio test set module and the front

panel assembly controls are shown in figures 6–4 through 6–20 The power supply schematic diagram is shown in figure 6–21.

3-4. Component Location Illustrations

To aid in troubleshooting the test set, the location of connectors, modules, and terminal boards are shown in figure 3–1① and ②. Exploded views of components that are replaceable at direct support level are provided in section IV.

3-5. Voltage and Resistance Measurements

CAUTION

Before attempting to perform voltage

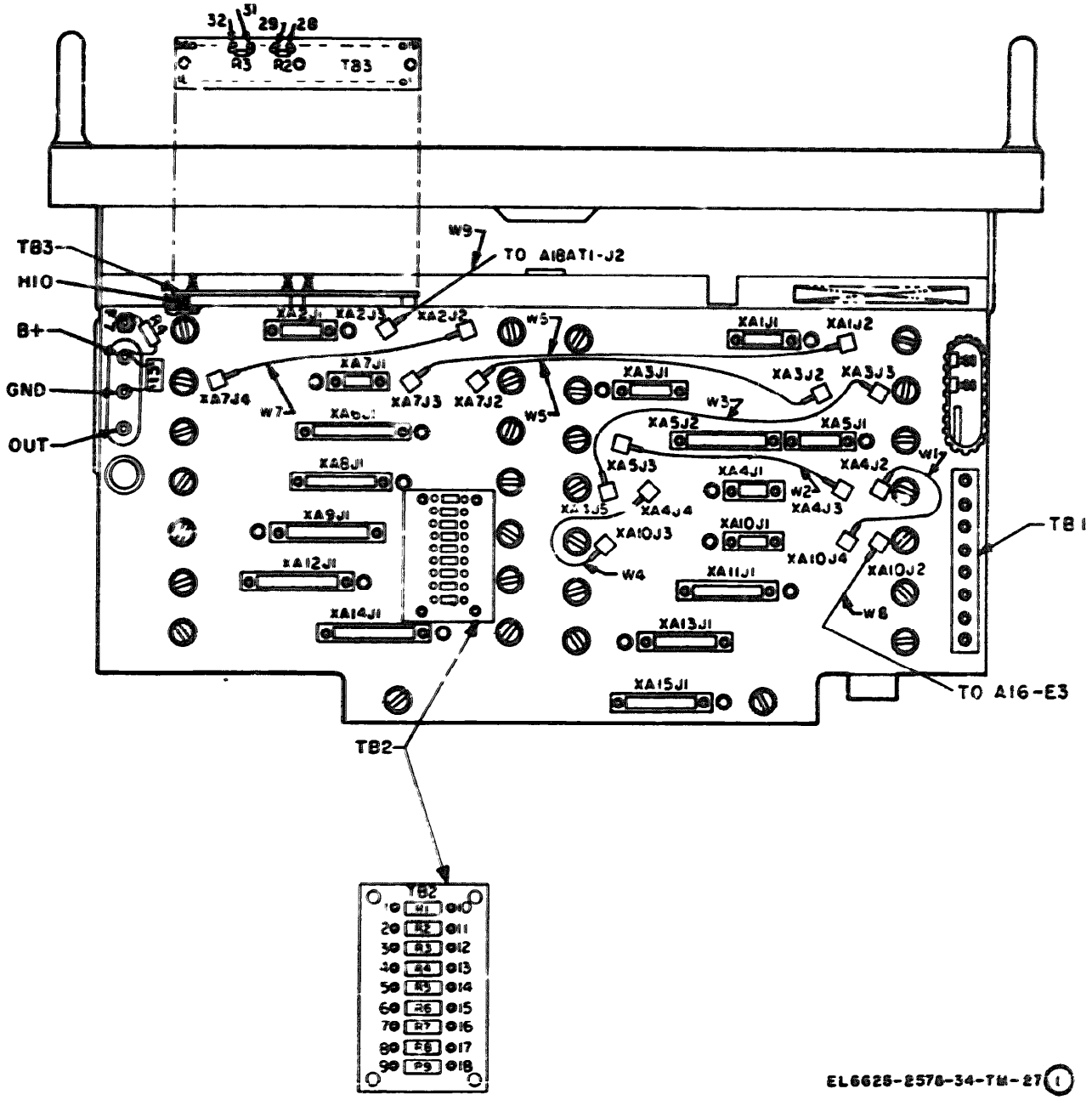
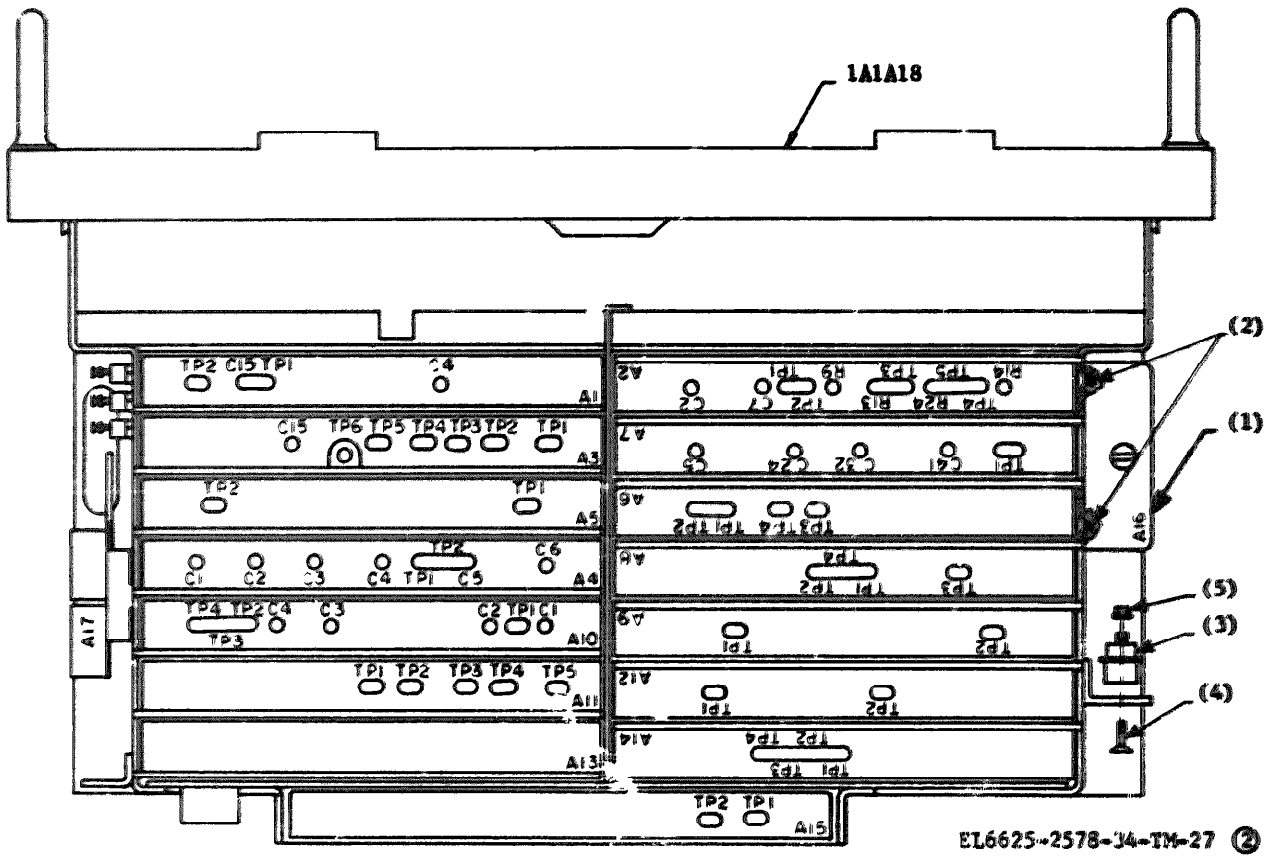



Figure 3-1 (1). Test set front panel module assembly, component location diagram (part 1 of 2).




1 Module 1A1A16
2 Flathead screw (2)
3 Connector 1A1P1
4 Flathead screw (2)
5 Retainer nut (2)

Figure 3-1(2). Test set front panel module assembly, component location diagram (part 2 of 2).

and resistance measurements, review the applicable voltage and resistance chart. Carefully follow instructions and observe notes on voltage and resistance charts. Carelessness may damage transistors or other sensitive circuit elements and make troubleshooting more difficult. *Do not remove or insert plug-in assemblies with voltage applied to the circuit.*

*a. General.* Before taking voltage and resistance measurements, the center housing assembly 1A2 must be removed and an extender cable connected between the center housing and front, and module assemblies power plug. Refer to paragraph 3–13 for disassembly instructions of the center housing assembly. Refer to paragraph 3–8 for fabrication instructions of the extender cable and figure 3–2 for the general equipment setup with extender cable.

*b. Test Conditions.* Voltage and resistance measurements in charts 3–1 through 3–4 were taken with a known good test set under normal operating conditions for voltage and with power removed for resistance. All measurements were referenced to chassis ground and were taken with a TS–352B/U multimeter. The equipment is connected as shown in figure 3–3. Unless otherwise noted, all voltage and resistance measurements represent typical measurements on a test set. Voltage tolerances are ±10% and resistance tolerances are ±20%.

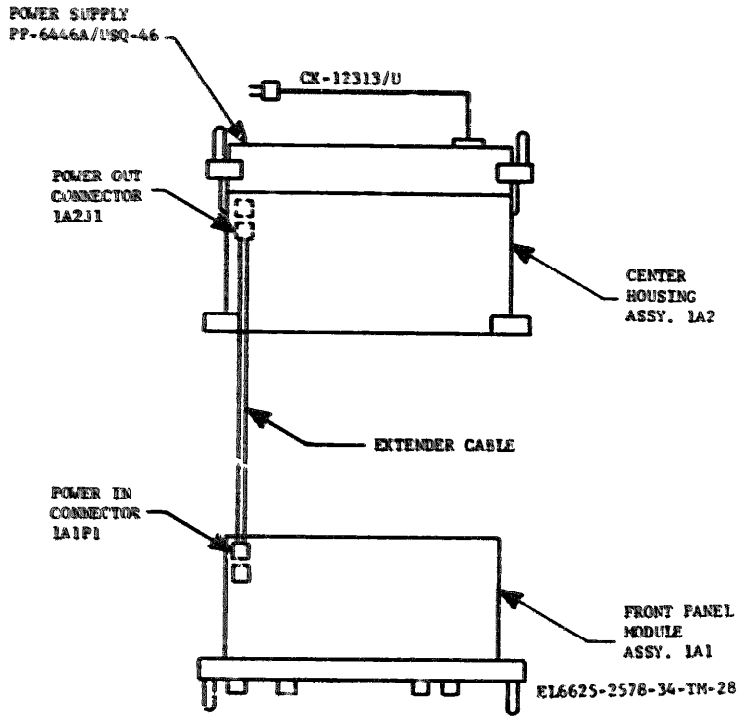



Figure 3-2. General equipment test setup.

Chart 3-1. Power Supply/Regulator 1A1A17 (fig 3-1(2)).

| Terminal | Volts dc | + Ohms |
|---|---|---|
| E1 | 12.0–16.0 | 26 |
| E2 | 5.0 | 6.3 k |
| E3 | 0 | 58 |
| E4 | 3.6 | 3.0 k |
| E5 | 7.2 | 0 |
| E6 | 10.0 | 3.0 k |
| E7 | 10.0 | 32 |

N O T E

**Voltage and resistance measurements were obtained with the equipment off for resistance data and with nominal 115 vac input to the power supply for voltage data.**

Chart 3-2. Terminal Board 1A1TB1 (fig. 3-1(1)).

| Terminal | Volts dc | + Ohms | – Ohms |
|---|---|---|---|
| 1 | 10.0 ± | 70 | 70 |
| 2 | 7.2 ± | 110 | 110 |
| 3 | 7.2 ± | 110 | 110 |
| 4 | 7.2 ± | 110 | 110 |
| 5 | 5.0 ± | 420 | 270 |
| 6 | – | | |

N O T E

**Voltage and resistance measurements were obtained with the equipment off for resistance data and with nominal 115 vac input to the power supply for voltage data. Channel switches were set for channel 1045, all other switches to any position.**

Chart 3-3. Terminal Board 1A1TB2 (fig. 3-1(1)).

| Terminal | Volts dc | + Ohms |
|---|---|---|
| 1 | 7.08 ± 0.03 | 3194 |
| 2 | 4.67 ± 0.03 | 2154 |
| 3 | 4.67 ± 0.03 | 2154 |
| 4 | 3.05 ± 0.02 | 1410 |
| 5 | 3.05 ± 0.02 | 1410 |
| 6 | 2.00 ± 0.01 | 917 |
| 7 | 2.00 ± 0.01 | 917 |
| 8 | 1.28 ± 0.01 | 576 |
| 9 | 1.28 ± 0.01 | 576 |
| 10 | 5.73 ± 0.03 | 2618 |
| 11 | 5.73 ± 0.03 | 2618 |
| 12 | 3.77 ± 0.02 | 1742 |
| 13 | 3.77 ± 0.02 | 1742 |
| 14 | 2.48 ± 0.02 | 1143 |
| 15 | 2.48 ± 0.02 | 1143 |
| 16 | 1.61 ± 0.01 | 730 |
| 17 | 1.61 ± 0.01 | 730 |
| 18 | 0 | 0 |

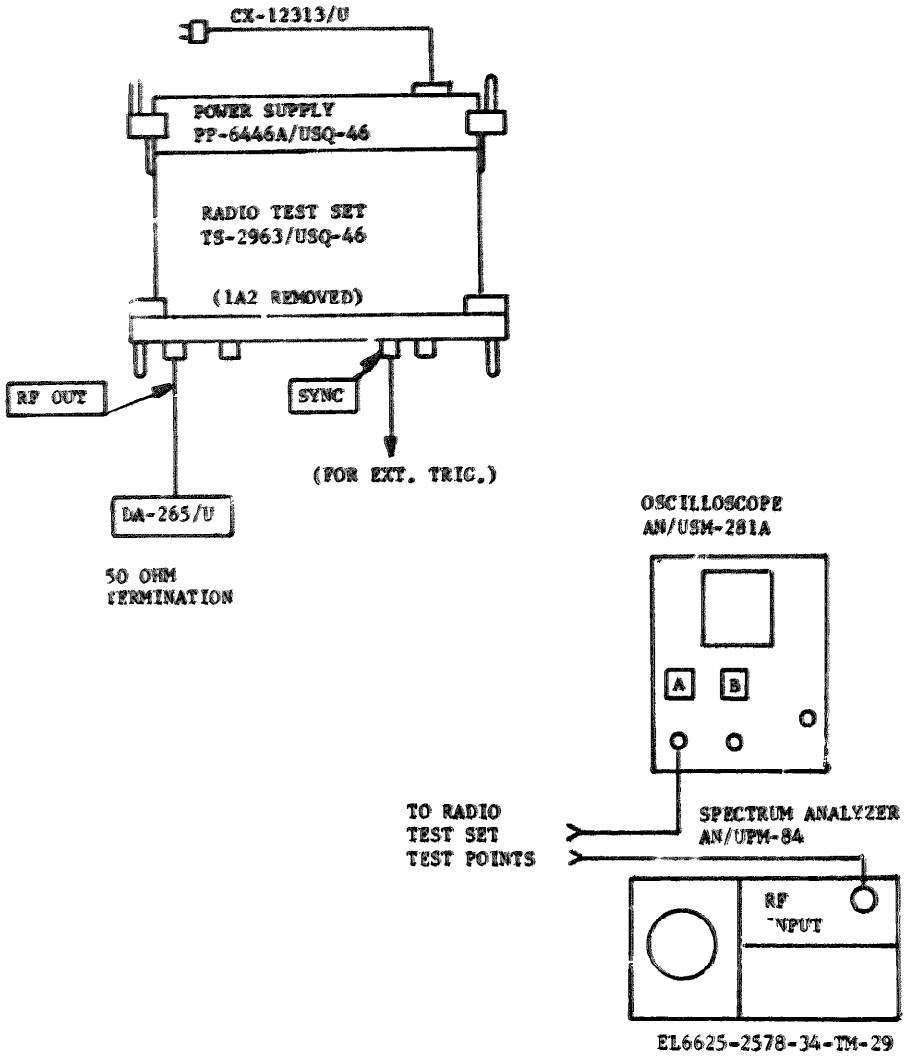



Figure 3-3. Voltage, resistance, and waveform troubleshooting test setup.

NOTE

Voltage and resistance measurements were obtained with the equipment off for resistance data and with nominal 115 vac input to the power supply for voltage data. Channel switches were set for channel 1045, all other switches to any position.

Chart 3-4. Terminal Board 1A1TB3 (fig. 3-1 (1)).

| Terminal | Volts dc | + Ohms |
|---|---|---|
| 1 | - | 1160 |
| 2 | - | - |
| 3 | - | 1100 |
| 4 | - | 1100 |
| 5 | 7.2 | 1080 |
| 6 | 7.2 | 1080 |
| 7 | - | 1100 |
| 8 | - | 1100 |
| 9 | 3.9 | 1000 |
| 10 | 3.9 | 1000 |
| 11 | 3.9 | 1000 |
| 12 | 3.8 | 1040 |
| 13 | 3.8 | 1040 |
| 14 | - | 900 |
| 15 | - | 900 |
| 16 | - | 900 |
| 17 | 3.8 | 1020 |
| 18 | 3.2 | 1020 |
| 19 | 7.2 | 1020 |
| 20 | 7.2 | 1020 |
| 21 | - | 1000 |
| 22 | - | 1000 |

| Terminal | Volts dc | + Ohms |
|---|---|---|
| 23 | - | 1060 |
| 24 | 6.0 | 1060 |
| 25 | 3.2 | 900 |
| 26 | - | 1020 |
| 27 | 10.0 | 40 |
| 28 | 5.2 | 450 |
| 29 | - | - |
| 30 | 7.2 | 110 |
| 31 | - | 1100 |
| 32 | - | 15 k |
| 33 | 3.8 | 1020 |
| 34 | - | 980 |
| 35 | 3.8 | 1050 |
| 36 | 3.8 | 1050 |

NOTE

Voltage and resistance measurements were obtained with the equipment off for resistance data and with 12.0 ±1.0 vdc input at 1A2P1 for voltage data. Channel switches were set for channel 1045, all other switches to any position.

## 3-6. Waveform Analysis

*a.* All system level test points are located on top of the plug-in modules. Waveforms and test point data are primarily intended for use in isolating faults to a given module with repair being limited to module replacement. Waveforms are not intended to be used for system alinement or calibration. Refer to paragraph 3-5b for general instructions on equipment test setup to obtain access to the modules, and to figure 3-1 for the module location. The specific test setup for evaluating waveform and test point data is shown in figure 3-3. The applicable test setup data is referenced under each test point callout as well as test equipment control settings.

*b.* The normal waveforms that should be observed at test points are shown in figure 3-4. By comparing observed waveforms with the normal waveforms, a trouble can be quickly located to a section or a faulty module.

*c.* Before comparing the observed waveforms with the normal waveforms, carefully read the notes on the waveform illustrations and exactly duplicate the conditions under which the normal waveforms were obtained.

*d.* When a waveform at a certain test point is observed to be abnormal, the cause may be the absence of a signal from another module. It is therefore advisable to check all inputs to the module where the abnormal waveform is observed as a first step in isolating a faulty module.

*e.* Chart 3-5 lists the test setup data notes used to obtain the system test point waveforms. The equipment test setup used to obtain these waveforms is shown in figure 3-3.

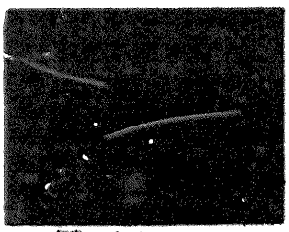
Chart 3-5. Test Set Waveform Notes.

| Note | Mode | Chnl | Prog | Mag | FSK | Meter | Atten | Remarks |
|---|---|---|---|---|---|---|---|---|
| 1 | INT | 1045 | Any | Any | W/F or W/S | Any | Any | Use oscilloscope |
| 2 | INT | 1045 | Any | Any | N/F or N/S | Any | Any | Use oscilloscope |
| 3 | REP A | 1045 | 01 | 1 | W/F or N/F | Any | Any | Use oscilloscope |
| 4 | REP A | 1045 | 01 | 1 | W/F | Any | Any | Use oscilloscope |
| 5 | REP A | 1045 | 01 | 1 | N/F | Any | Any | Use oscilloscope |
| 6 | REP A | 1045 | 01 | 1 | W/S | Any | Any | Use oscilloscope |
| 7 | REP A | 1045 | 01 | 1 | N/S | Any | Any | Use oscilloscope |
| 8 | CAL | 1045 | Any | Any | Any | Any | Any | Use oscilloscope |
| 9 | CAL | 0001 and 0299 | Any | Any | Any | Any | Any | Use oscilloscope |
| 10 | See Waveform | 1045 | 01 | 1 | W/F or N/F | Any | Any | Use oscilloscope |
| 11 | REP M | 1045 | 01 | 1 | W/F | Any | Any | Use oscilloscope |
| 12 | REP A | 1045 | 01 | 1 | N/F or W/S | Any | Any | Use oscilloscope |

| Mode | Chnl | Prog | Mag | PSK | Meter | Atten | Remarks |
|---|---|---|---|---|---|---|---|
| See Waveform | 1045 | 01 | 1 | W/S or N/S | Any | Any | Use oscilloscope |
| REP M INT | 1045 | 01 | 4 | W/F | Any | Any | Use oscilloscope |
| SEQ A | 1045 | 01 | 1 | W/F | Any | Any | Use oscilloscope |
| CAL | 1045 | Any | Any | Any | Any | Any | Use spectrum analyzer. |

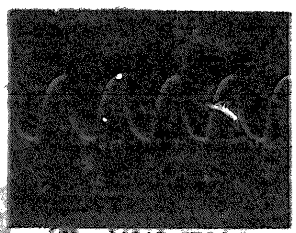
(C) 1A1A1-TP2(a)
SEE NOTE 1
VERT: 0.5V/cm
SWEEP: 0.5 ms/cm
SYNC: INT
PROBE: X1
INPUT: AC Coupled

(C) 1A1A1-TP2(b)
SEE NOTE 2
VERT: 0.5V/cm
SWEEP: 0.5 ms/cm
SYNC: INT
PROBE: X1
INPUT: AC Coupled

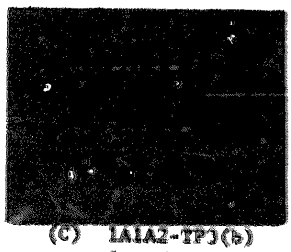


(U) 1A1A2-TP1
See Note 3
VERT: 0.2V/cm
SWEEP: 10 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: AC Coupled

(U) 1A1A2-TP2
See Note 3
VERT: 0.2V/cm
SWEEP: 10 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: AC Coupled



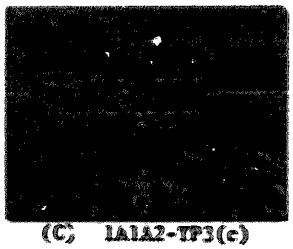
(C) 1A1A2-TP3(a)
See Note 4
VERT: 0.5V/cm
SWEEP: 0.5 ms/cm
SYNC: INT
PROBE: X1
INPUT: AC Coupled



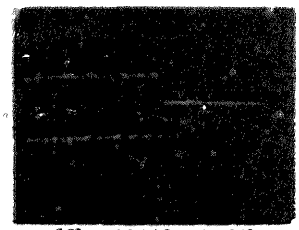
(C) 1A1A2-TP3(b)
See Note 4
VERT: 0.5V/cm
SWEEP: 10 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: AC Coupled

EL6625-2578-34-TM-30(1)

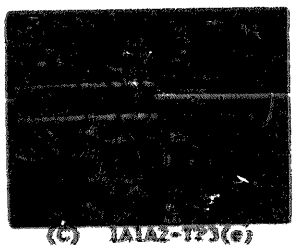
Figure 3-4(1). Test set system waveforms (part 1 of 10).



(C) 1A1A2-TP3(c)
See Note 5
VERT: 0.5V/cm
SWEEP: 10 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: AC Coupled



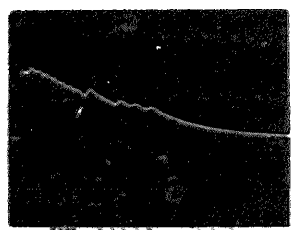
(C) 1A1A2-TP3(d)
See Note 6
VERT: 0.5V/cm
SWEEP: 50 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: AC Coupled



(C) 1A1A2-TP3(e)
See Note 7
VERT: 0.5V/cm
SWEEP: 50 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: AC Coupled

(U) 1A1A2-TP4(a)
See Note 4
VERT: 20 mv/cm
SWEEP: 20 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: AC Coupled

(U) 1A1A2-TP4(b)
See Note 5
VERT: 20 mv/cm
SWEEP: 20 ms/cm
SYNC: EXT (from Test Set)
PROBE: X1
INPUT: AC Coupled



(U) 1A1A2-TP4(c)
See Note 6
VERT: 20 mv/cm
SWEEP: 20 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: AC Coupled

EL6625-2578-34-TM-30

Figure 3-4(1). Test set system waveforms (part 2 of 10).

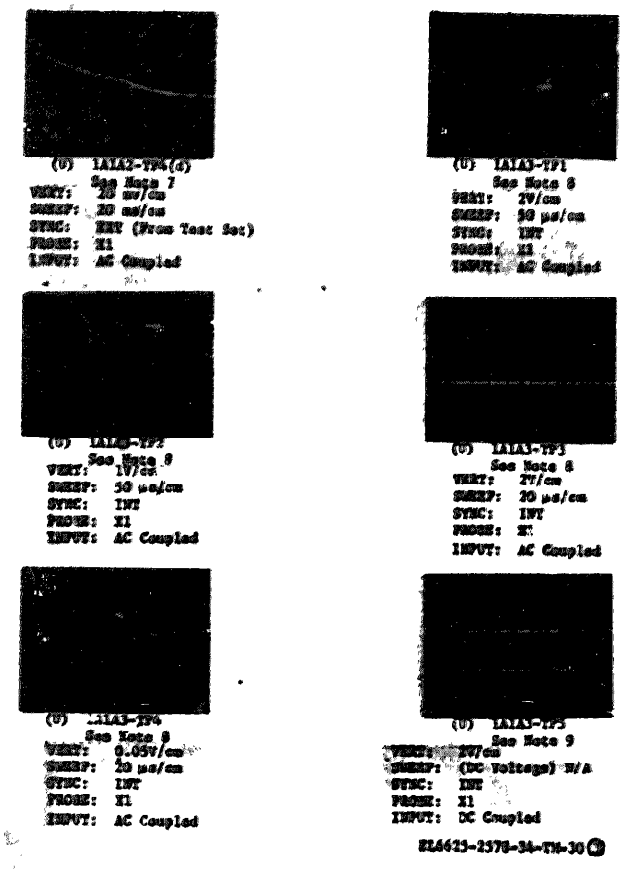
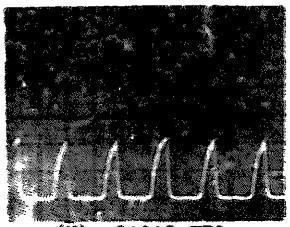
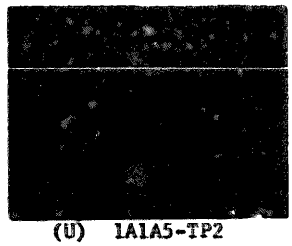


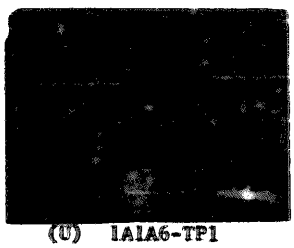

Figure 3-4(3). Test set system waveforms (part 3 of 10).



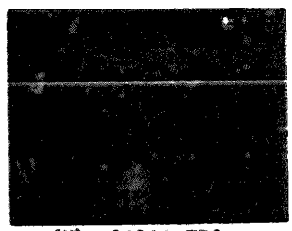
(U) 1A1A5-TP1
See Note 8
VERT: 2V/cm
SWEEP: 0.2 µs/cm
SYNC: INT
PROBE: X1
INPUT: AC Coupled



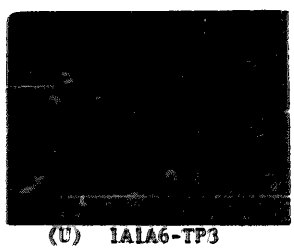
(U) 1A1A5-TP2
See Note 8
VERT: 2V/cm
SWEEP: 20 µs/cm
SYNC: INT
PROBE: X1
INPUT: AC Coupled



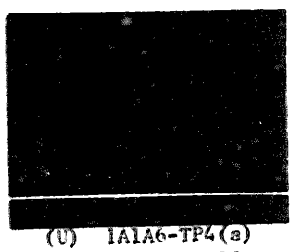
(U) 1A1A6-TP1
See Note 11
VERT: 2V/cm
SWEEP: 0.2 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled



(U) 1A1A6-TP2
See Note 4
VERT: 2V/cm
SWEEP: 10 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled



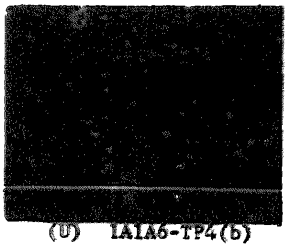
(U) 1A1A6-TP3
See Note 10
VERT: 2V/cm
SWEEP: 0.5 ms/cm
SYNC: INT
PROBE: X1
INPUT: DC Coupled



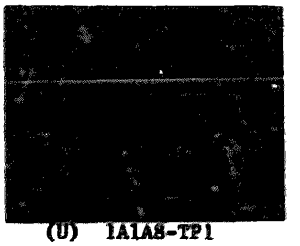
(U) 1A1A6-TP4(a)
See Note 12
VERT: 2V/cm
SWEEP: 50 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled

EL6625-2578-34-TM-30 (4)

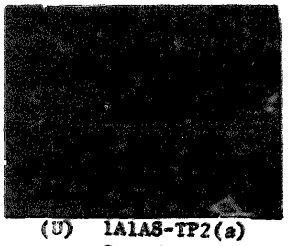
Figure 3-4(4). Test set system waveforms (part 4 of 10).



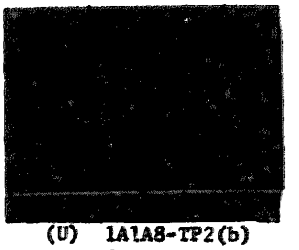
(U) 1A1A6-TP4(b)
See Note 3
VERT: 2V/cm
SWEEP: 50 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled



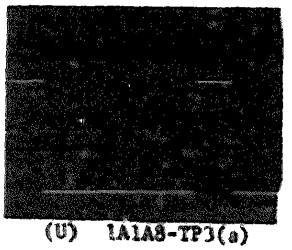
(U) 1A1A8-TP1
See Note 4
VERT: 2V/cm
SWEEP: 0.2 sec/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled



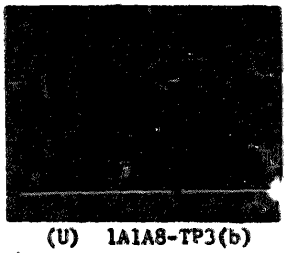
(U) 1A1A8-TP2(a)
See Note 10
VERT: 2V/cm
SWEEP: 10 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled



(U) 1A1A8-TP2(b)
See Note 13
VERT: 2V/cm
SWEEP: 50 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled



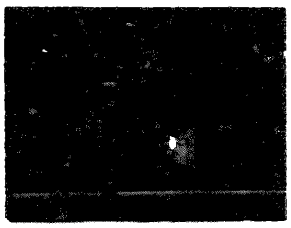
(U) 1A1A8-TP3(a)
See Note 12
VERT: 2V/cm
SWEEP: 0.2 sec/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled



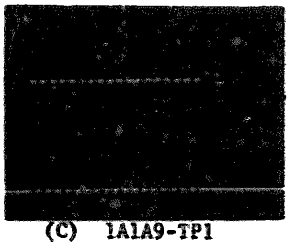
(U) 1A1A8-TP3(b)
See Note 4
VERT: 2V/cm
SWEEP: 0.2 sec/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled

EL6625-2578-34-TM-30 (5)

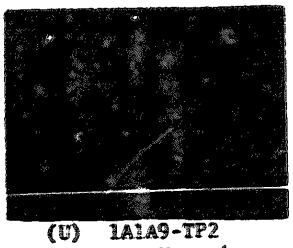
Figure 3-4(5). Test set system waveforms (part 5 of 10).



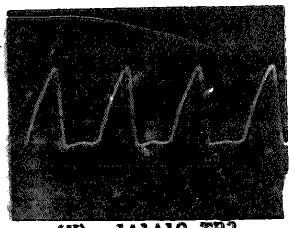
(U) 1A1A8-TP4
See Note 4
VERT: 2V/cm
SWEEP: 2 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled



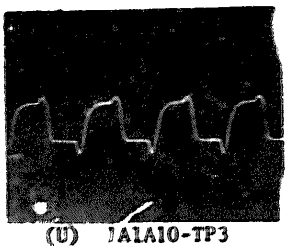
(C) 1A1A9-TP1
See Note 4
VERT: 2V/cm
SWEEP: 10 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled



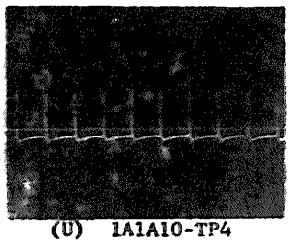
(U) 1A1A9-TP2
See Note 4
VERT: 2V/cm
SWEEP: 10 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled



(U) 1A1A10-TP2
See Note 8
VERT: 1V/cm
SWEEP: 0.1 µs/cm
SYNC: INT
PROBE: X1
INPUT: AC Coupled



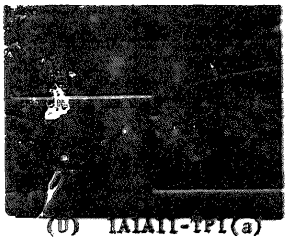
(U) 1A1A10-TP3
See Note 8
VERT: 5V/cm
SWEEP: 0.2 µs/cm
SYNC: INT
PROBE: X1
INPUT: AC Coupled



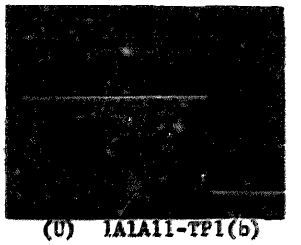
(U) 1A1A10-TP4
See Note 8
VERT: 0.5V/cm
SWEEP: 0.5 µs/cm
SYNC: INT
PROBE: X1
INPUT: AC Coupled

EL6625-2578-34-TM-30

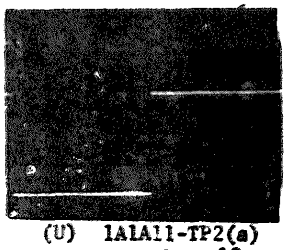
Figure 3-4(6). Test set system waveforms (part 6 of 10).



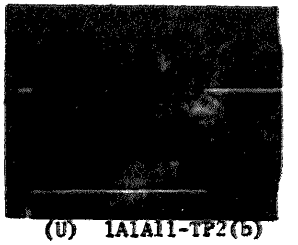
(U) 1A1A11-TP1(a)
See Note 12
VERT: 2V/cm
SWEEP: 50 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled



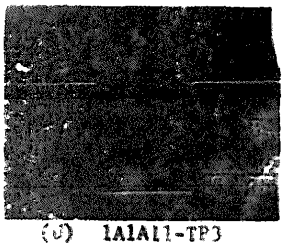
(U) 1A1A11-TP1(b)
See Note 3
VERT: 2V/cm
SWEEP: 10 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled



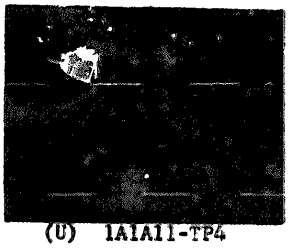
(U) 1A1A11-TP2(a)
See Note 12
VERT: 2V/cm
SWEEP: 50 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled



(U) 1A1A11-TP2(b)
See Note 3
VERT: 2V/cm
SWEEP: 10 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled



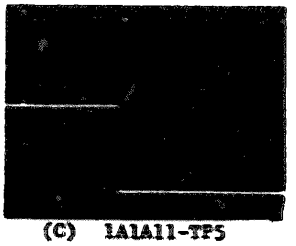
(U) 1A1A11-TP3
See Note 3
VERT: 2V/cm
SWEEP: 1 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled



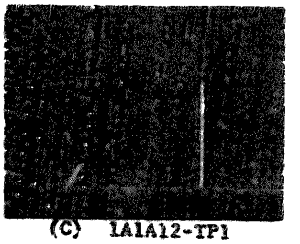
(U) 1A1A11-TP4
See Note 3
VERT: 2V/cm
SWEEP: 1 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled

EL6625-2578-34-TM-30 (7)

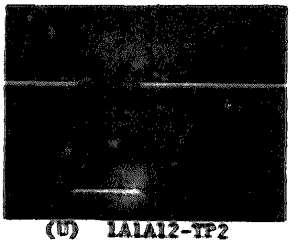
Figure 3-4(7). Test set system waveforms (part 7 of 10).



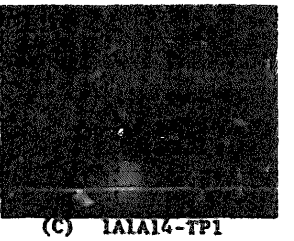
(C) 1A1A11-TP5
See Note 14
VERT: 2V/cm
SWEEP: 5 sec/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled



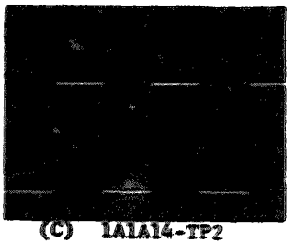
(C) 1A1A12-TP1
See Note 15
VERT: 2V/cm
SWEEP: 10 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled



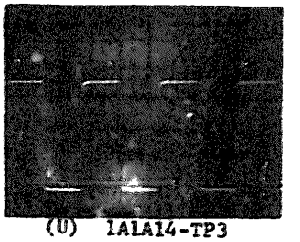
(U) 1A1A12-TP2
See Note 15
VERT: 2V/cm
SWEEP: 0.5 sec/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled



(C) 1A1A14-TP1
See Note 15
VERT: 2V/cm
SWEEP: 10 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled



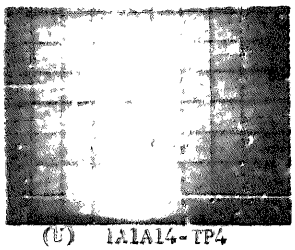
(C) 1A1A14-TP2
See Note 15
VERT: 2V/cm
SWEEP: 0.5 ms/cm
SYNC: INT
PROBE: X1
INPUT: AC Coupled



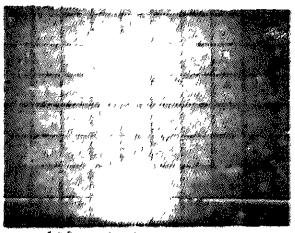
(U) 1A1A14-TP3
See Note 15
VERT: 2V/cm
SWEEP: 20 µs/cm
SYNC: INT
PROBE: X1
INPUT: AC Coupled

LL6625-2578-34-TM-30

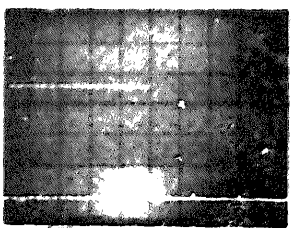
Figure 3-4(8). Test set system waveforms (part 8 of 10).



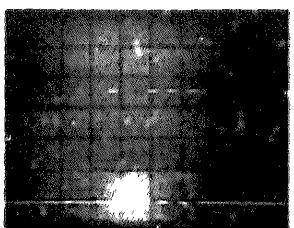
(U) 1A1A14-TP4
See Note 15
VERT: 2V/cm
SWEEP: 10 ms/cm
SYNC: INT
INPUT: DC Coupled



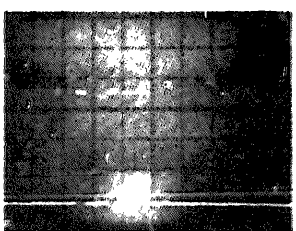
(C) 1A1A15-TP1(a)
See Note 3
VERT: 2V/cm
SWEEP: 10 ms/cm
SYNC: EXT (From Test Set)
INPUT: DC Coupled



(C) 1A1A15-TP1(b)
See Note 12
VERT: 2V/cm
SWEEP: 10 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled



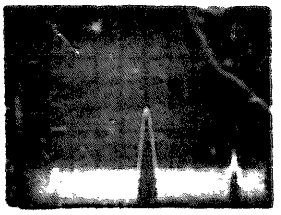
(U) 1A1A15-TP2(a)
See Note 3
VERT: 2V/cm
SWEEP: 10 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled



(U) 1A1A15-TP2(b)
See Note 12
VERT: 2V/cm
SWEEP: 50 ms/cm
SYNC: EXT (From Test Set)
PROBE: X1
INPUT: DC Coupled

EL6625-2578-34-TM-30 (9)

Figure 3-4(9). Test set system waveforms (part 9 of 10).



(U) 1A1A4-TP1
See Note 16

| | |
|---|---|
| PROBE: | X1 |
| BW: | 100 kHz |
| SCANWIDTH: | 0.5 MHz/div |
| INPUT ATTEN: | 10 dB |
| VIDEO FILTER: | OFF |
| SCAN TIME: | 1 ms/div |
| LOG REF LEVEL: | -10 dB |
| LIN SENS: | -3 dB |
| SCAN MODE: | INT |
| SCAN TRIG: | AUTO |
| LOG LINEAR SW: | LOG |

(U) 1A1A4-TP2
See Note 16

| | |
|---|---|
| PROBE: | X1 |
| BW: | 100 kHz |
| SCANWIDTH: | 0.5 MHz/div |
| INPUT ATTEN: | 10 dB |
| VIDEO FILTER: | OFF |
| SCAN TIME: | 1 ms/div |
| LOG REF LEVEL: | -10 dB |
| LIN SENS: | - 3 dB |
| SCAN MODE: | INT |
| SCAN TRIG: | AUTO |
| LOG LINEAR SW: | LOG |

EL6625-2578-34-TM-30 (10)

Figure 3-4(10). Test set system waveforms (part 10 of 10).

## S e c t i o n I I .

### 3-7. Tools, Materials, and Equipment

**All tools, materials, and test equipment required to perform testing procedures in this chapter are listed below.**

***a. Tools.***

**NOTE**

**Tools contained in the TK-100/G are listed in Department of the Army Supply Catalog SC 5180-91-CL-S21.**

| *Quantity* | *Item* |
|---|---|
| 1 | Toolkit, Electronics Equipment TK-100/G. |

***b. Materials.***

| *Quantity* | *Item* |
|---|---|
| As required | Silicone lubricant, Dow Corning #7. |
| As required | Wire, copper, insulated, 20 AWG. |
| 1 | Cannon connector DEM-9P (same as 1A1P1). |
| 1 | Cannon connector DEM-9S (same as 1A2A2J1). |

***c. Test Equipment.***

| *Test equipment** | *Common name* |
|---|---|
| Power Supply PP-3940A/G. | Power supply |
| Oscilloscope AN/USM-281A. | Oscilloscope |
| RF Frequency Counter AN/USM-207. | Frequency counter |
| Spectrum Analyzer AN/UPM-84. | Spectrum analyzer |
| RF Voltmeter (with 50-ohm probe) AN/URM-145. | RF voltmeter |
| Headset H-251/U | Headset |
| RF Monitor R-1617A/USQ-46. | RF monitor |
| RF Indicator ID-1721/USQ-46. | RF indicator |

*Or equivalent.

### 3-8. Fabrication of Extender Cable

An extender cable is required when troubleshooting the test set. This cable provides power input to the radio test set when the center housing which contains the input power connector, is re

moved to provide access to the modules. Fabricate the cable from materials listed in paragraph 3-7*b* according to the extender cable diagram (fig. 3-5).

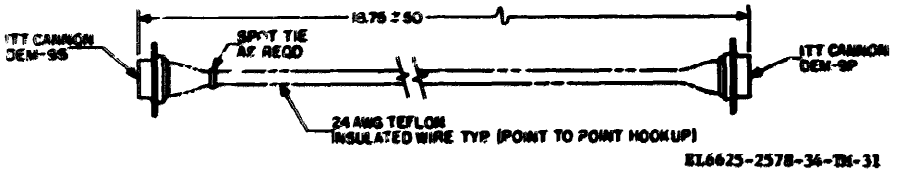



Figure 3-5. Extender cable fabrication diagram.

## Section III. DIRECT SUPPORT TROUBLESHOOTING OF THE TEST SET

### 3-9. Troubleshooting Procedures

*a. General.* To be effective, troubleshooting must by systematic. It is seldom possible to observe a trouble symptom and immediately diagnose the cause. If a systematic sequence is followed, a trouble will first be isolated to a section and then to a module or subassembly within that section.

b. Sectionalization. A trouble may be sectionalized by performing visual checks operational tests (TM 11-6625-2578-12), and by use of a troubleshooting chart and the overall functional block diagram (fig. 6-3).

c. Isolation. Trouble isolation may be accomplished by performing voltage and resistance checks (para 3-5) and test point waveform comparisons (para 3-6).

*d. Faulty Module or Component.* When a trouble has been isolated to a faulty module, replace the module (sec. IV) and forward the faulty module to depot maintenance. When a trouble has been isolated to a faulty component, replace the component (sec. IV) if it is replaceable at the direct support level or forward the test set to ground support maintenance.

### 3-10. Troubleshooting Chart

Perform sectionalization and isolation procedures as defined in paragraph 3-9 using the troubleshooting chart below.

Chart 3-6. Direct Support Test Set Troubleshooting Chart

| Item No. | Trouble symptom | Probable trouble, checks, corrective measures |
|---|---|---|
| 1 | No front panel meter movement indicated when MODE switch is in CAL position, METER switch is RF LEVEL position and LEVEL SET control rotated fully clockwise. | *a.* Power input circuit open. Check MODE switch 1A1A18-S7 and METER switch 1A1A18-S10 (fig. 3-7), connectors 1A1P1 (fig. 3-1) and 1A2J1 (fig. 3-9), and fuze 1A1A18-F1 or fuse holder 1A1A18-XF1 (fig. 3-7) Replace defective component.<br>*b.* Faulty power supply/regulator (1A1A17), VCXO (1A1A1), detector output (1A1A2), RF mixer amplifier (1A1A7), loop filter/VCO (1A1A3), synthesizer mixer (1A1A4), or reference generator (1A1A10) module (fig. 3-1). Replace faulty module.<br>*c.* Faulty Power Supply PP-6446A/USQ-46. Replace if defective.<br>*d.* Defective meter 1A1A18M1. Next higher category of maintenance required. |
| 2 | No front panel meter movement indicated when MODE switch in INT position, METER switch in DEV position, and DEV control rotated fully clockwise. | *a.* Faulty VCXO (1A1A1) or detector output (1A1A2), module (fig. 3-1). Replace faulty module.<br>*b.* Check MODE switch 1A1A18-S7 and METER switch 1A1A18-S10 (fig. 3-1) and replace if defective. |
| 3 | Proper front panel meter indication with MODE switch in INT position but no audio in headset connected to RF Monitor R-1617A/USQ-46. | *a.* Faulty VCXO (1A1A1), TCXO (1A1A16), synthesizer/mixer (1A1A4), loop filter/VCO (1A1A3), programable divider (1A1A5) or reference generator (1A1A10) module (fig. 3-1). Replace faulty module.<br>*b.* Check METER switch 1A1A18-S10 (fig. 3-7) and replace if defective. |
| 4 | No output indicated on front panel meter when START switch is pressed and with MODE switch in SEQ A, SEQ M, REP A, or REP M position. | *a.* Check START switch 1A1A18-S11 (fig. 3-7) and replace if defective.<br>*b.* Faulty word length generator (1A1A9), mode control I (1A1A6), mode control II (1A1A8), mode control III (1A1A11) or VCXO (1A1A1) module (fig. 3-1). Replace faulty module.<br>*c.* Check METER switch 1A1A18-S10 (fig. 3-7) and replace if defective. |

| Item No. | Trouble symptom | Probable trouble, checks, corrective measures |
|---|---|---|
| 5 | No coding displayed on RF Monitor R-1617A/USQ-46 when MODE switch in SEQ A, SEQ M, REP A or REP M position. | a. Check FSK switch 1A1A18-S8 (fig. 3-7) for proper position (W/F or W/S).<br>b. Check front panel attenuator switches for excessive attenuation.<br>c. Faulty mode control I (1A1A6), mode control II (1A1A8), mode control III (1A1A11), word length generator (1A1A9) or shift register (1A1A15 module (fig. 3-1). Replace faulty module. |
| 6 | Incorrect coding displayed on RF Monitor R-1617/USQ-46 with MODE switch in SEQ A or SEQ M position. | a. Check front panel attenuator switches for excessive attenuation.<br>b. Check FSK switch 1A1A18-S8 (fig. 3-7) for proper position (W/F or W/S).<br>c. Faulty word length generator (1A1A9), mode control I (1A1A6), Mode Control II (1A1A8), encoder I (1A1A12), encoder II (1A1A14), encoder matrix (1A1A13), or shift register (1A1A15) module fig. 3-1). Replace faulty module. |
| 7 | Incorrect coding displayed on RF Monitor R-1617A/USQ-46 with MODE switch in REP A or REP M position. | a. Check front panel attenuation switches for excessive attenuation.<br>b. Check FSK switch 1A1A18-S8 (fig. 3-7) for proper position (W/F or W/S).<br>c. Defective PROGRAM switches 1A1A18-S5 and S6. Replace defective switch.<br>d. Faulty encoder I (1A1A12), encoder II (1A1A14), encoder matrix (1A1A13), mode control I (1A1A6), or mode control II (1A1A8) module (fig. 3-1). Replace faulty module. |
| 8 | Improper audio output from RF Monitor R-1617A/USQ-46 with MODE switch in REP M and MESSAGE switch in type 4 position. | a. Faulty VCXO (1A1A1), mode control I (1A1A6), word length generator (1A1A9) or encoder I (1A1A12) module (fig. 3-1). Replace faulty module. |
| 9 | No external modulation capability | a. Check EXT MOD IN connector 1A1A18-J2 and MODE switch 1A1A18-S7 (fig. 3-7). Replace defective component.<br>b. Faulty VCXO (1A1A1) module (fig. 3-1). Replace if defective. |
| 10 | No SYNC output at 1A1A18-J4 | a. Check SYNC connector 1A1A18-J4 (fig. 3-7) and replace if defective.<br>b. Faulty mode control II (1A1A8) module (fig. 3-1). Replace if defective. |
| 11 | No video output at 1A1A18-J1 | a. Check VIDEO connector 1A1A18-J2 (fig. 3-7) and replace if defective.<br>b. Faulty word length generator (1A1A9) module (fig. 3-1). Replace if defective. |

## Section IV. DIRECT SUPPORT REMOVAL AND REPLACEMENT OF TEST SET COMPONENTS

### 3-11. General

**This section provides** detailed removal and replacement instructions for test set modules and **components that are replaceable at direct support level. When it is necessary to replace a component which is accessible without disassembling the entire equipment, perform only those steps necessary to reach that component.**

### 3-12. Removal or Replacement of Power Supply PP-6446A/USQ-46 (fig. 3-6).

a. Disassembly.

(1) Place test set (1) face downwards on handles.

(2) Pull latches (2) out and up from test set (1) to unlatch.

(3) Remove power supply (3) by lifting straight up.

b. Reassembly.

(1) Position power supply (3) in place on test set (1) and press down firmly.

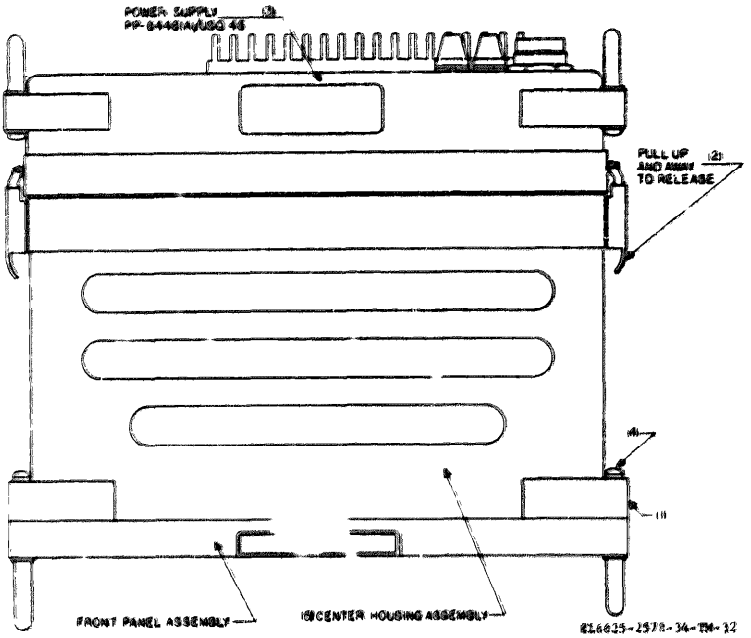
(2) Place latches (2) on power supply retaining hooks, press down and in to secure power supply (3) to test set (1).

### 3-13. Removal or Replacement of Center Housing 1A2 (fig. 3-6).

***a. Disassembly.***

(1) Perform step a of paragraph 3-12

(2) Loosen four captive screws (4) and pull center housing assembly (5) straight up to remove from front panel module assembly 1A1 (fig. 3-1).




1 Test Set TS 2963
2 Latches (2)
3 Power Supply PP-6446A
4 Captive screws (4)
5 Center housing assembly

Figure 3-6. Power supply and center housing assembly 1A2, removal or replacement..

*b. Reassembly.*

(1) Position center housing assembly (5) over front panel module assembly (fig. 3-1) and slide downwards slowly, but firmly.

(2) Tighten four captive screws (4) to secure center housing assembly (5).

(3) Perform step *b* of paragraph 3-12.

3-14. Removal or Replacement of Front Panel Assembly 1A1A18 (fig. 3-7).

*a. Disassembly.*

(1) Perform step *a* of paragraphs 3-12 and 3-13.

(2) Place the test set on a flat surface with the front panel assembly 1A1A18 (1) upright.

(3) Remove six seelskrews (2) located on the sides of (three on a side) the front panel assembly (1).

(4) Lay front panel assembly (1) forward on the handles to the limit of the cable service loop.

*b. Reassembly.*

(1) Position front panel assembly (1) to the upright position and align six holes in the sides of the front panel assembly with those on the front panel module assembly.

(2) Replace and tighten the six seelskrews (2).

(3) Perform step *b* of paragraphs 3-12 and 3-13.

3-15. Removal or Replacement of Front Panel Assembly 1A1A18 Environmental Gasket (fig. 3-7).

*a. Disassembly.*

(1) Perform step *a* of paragraphs 3-12, 3-13, and 3-14 in sequence.

CAUTION

Sharp tools should not be used when replacing gasket due to the possibility of damaging the gasket during insertion.

(2) Loosen and remove environmental gasket (3) from front panel assembly (1).

*b. Reassembly.*

(1) Apply silicone lubricant, specified in paragraph 3-7, to the new gasket (3) and gasket mounting area.

(2) Install new gasket (3) in gasket tray.

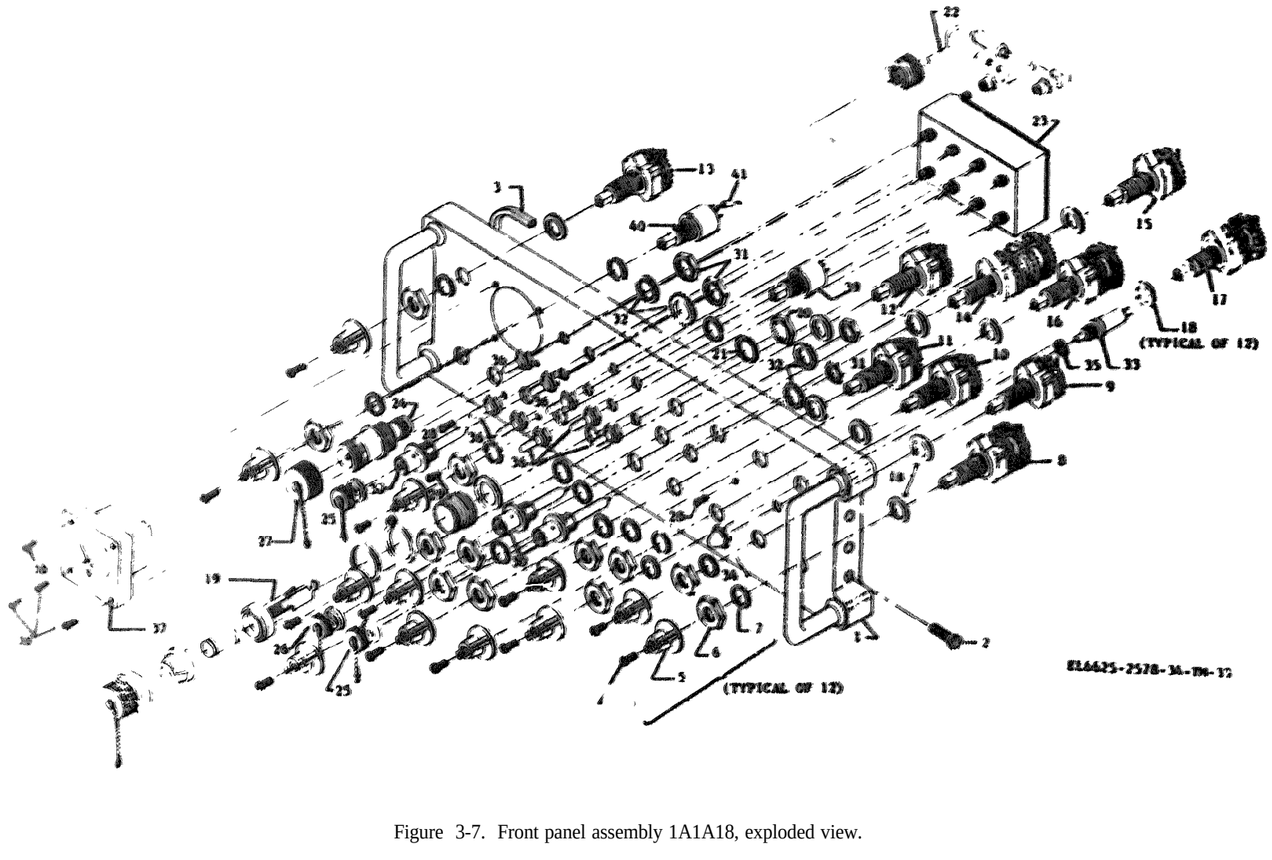



Figure 3-7. Front panel assembly 1A1A18, exploded view.

1 Front panel
2 Seelskrew (6)
3 Gasket
4 Panel screw
5 Knob
6 Retainer nut
7 Lockwasher
8 Mode switch
9 Message switch
10 FSK switch
11 Program switch
12 Channel switch
13 Meter switch
14 Channel switch
15 Program switch
16 Channel switch
17 Channel switch
18 O-ring
19 Fuse holder
20 Retaining nut
21 Lockwasher
22 Cable assembly
23 Attenuator assembly
24 Connector S3
25 Dustcap 81415-1
26 Dustcap 81415-3
27 Dustcap 9760-10
28 Panhead screw
30 Antenna connector
31 Retainer nut
32 Lockwasher
33 Start switch S-11
34 Retaining nut
35 Spacer
36 Waterseal boot and retainer nut (8)
37 Meter
38 Seelskrew
39 Level dev. control
40 Level set control
41 Resistor

Figure 3-7 -- Continued

(3) Perform step *b* of paragraphs 3–14, 3–13, and 3–12 in this sequence.

3-16. Removal or Replacement of Knobs for CHANNEL, MODE, MESSAGE, FSK, PROGRAM and METER Switches and Controls LEVEL SET and LEVEL DEV (fig. 3-7).

*a. Disassembly.* Remove panel screw (4) and remove knob (5).

*b. Reassembly.* Position knob (5) over shaft end of switch or control, replace and tighten screw (4).

3-17. Removal or Replacement of CHANNEL, PROGRAM, MODE, FSK, METER and MESSAGE Switches 1A1A18-S1 Through -S10 (fig. 3-7).

*a. Disassembly.*

(1) Perform step *a* of paragraphs 3–12 through 3–14, and 3–16 in sequence.

(2) Unsolder wires to applicable switch, noting terminal connection, and mark wires as required.

(3) Remove nut (6) and lockwasher (7) and remove applicable switch by pulling it from the rear of front panel assembly (1). Remove O-ring (18) from applicable switch. Items 6, 7, and 18 are supplied with each replacement switch and therefore need not be saved during removal.

*b. Reassembly.*

(1) Place O-ring (18) in seating space on applicable switch (items 8 through 17) and position switch in place on front panel assembly (1).

(2) Apply silicone lubricant as specified in paragraph 3–7, to switch and switch mounting area.

(3) Secure switch with lockwasher (7) and retaining nut (6).

(4) Solder wires to terminals, as marked during removal.

(5) Perform step *b* of paragraphs 3–16, 3–14, 3–13, and 3–12 in this sequence.

3-18. Removal or Replacement of Fuse Holder 1A1A18-XF1 (fig. 3-7).

*a. Disassembly.*

(1) Perform step *a* of paragraphs 3–12, 3–13, and 3–14 in sequence.

(2) Unsolder wires to fuse holder (19) noting terminal connections, and mark wires as required.

(3) Remove retaining nut (20) and lockwasher (21) and remove fuseholder (19) by pulling it out from the face of the front panel assembly (1). Items 20 and 21 are supplied with replacement fuse holders and therefore need not be saved during removal.

*b. Reassembly.*

(1) Apply silicone lubricant, as specified in paragraph 3–7, to mounting area of fuse holder (19) and front panel assembly (1).

(2) Place fuse holder (19) in position and secure with lockwasher (21) and retaining nut (20).

(3) Solder wires to fuse holder terminals, as marked during removal.

(4) Perform step *b* of paragraphs 3–14, 3–13, and 3–12 in this sequence.

3-19. Removal or Replacement of Cable Assembly 1A1A18W1 (fig. 3-7).

*a. Disassembly.*

(1) Perform step *a* of paragraphs 3–12 and 3–13 in sequence.

(2) Remove cable assembly (22) by loosening (counterclockwise) connector nuts at each end of cable.

*b. Reassembly.*

(1) Position cable assembly (22) at attenuator (23) and connector 1A1A18–S3 (24) and secure by tightening connector nuts.

(2) Perform step *b* of paragraphs 3–13 and 3–12 in this sequence.

3-20. Removal or Replacement of Connector Dust Caps (fig. 3-7).

*a. Disassembly.* Remove dust caps (25, 26 or 27) by twisting counterclockwise and then removing panhead screws (28 or 29) securing the dust cap retaining chains.

*b. Reassembly.* Position dust caps (25, 26 or 27) over appropriate connector and secure to connector by twisting clockwise. Secure dust cap retaining chain with panhead screws (28 or 29)

3-21. Removal or Replacement of Front Panel Assembly Connectors 1A1A18-J1, -J2, -J3 and -J4 (fig. 3-7).

*a. Disassembly.*

(1) Perform step *a* of paragraphs 3-12, 3–13, and 3–14 in sequence.

(2) Unsolder wires to connector 1A1A18–J1, –J2 or –J4 (30) or disconnect cable assembly (22) from 1A1A18–J3 (24).

(3) Remove retaining nut (31) and lockwasher (32) to remove connector 1A1A18–J1, –J2, or –J4 (30) or connector 1A1A18–J3 (24). Items 31 and 32 are supplied with replacement parts and therefore need not be saved.

*b. Reassembly.*

(1) Apply silicone lubricant, specified in paragraph 3–7, to mounting area of connectors (30 or 34) and front panel assembly (1).

(2) Position connector 1A1A18–J1, –J2 or –J4 (3) or connector 1A1A18–J3 (24) in appropriate slot in front panel assembly (1) and secure with lockwasher (32) and retaining nut (31).

(3) Solder wire to appropriate connector 1A1A18–J1, –J2, or –J4 (30) or connector cable assembly (22) to connector 1A1A18–J3 (24).

(4) Perform step *b* of paragraphs 3–14, 3–13, and 3–12 in this sequence.

3-22. Removal or Replacement of Front Panel Assembly START Switch 1A1A18-S11 and Its Waterseal Boot (fig. 3-7).

*a. Disassembly.*

(1) Perform step *a* of paragraphs 3–12, 3–13, and 3–14.

(2) Unsolder wires to switch (33) noting terminal connections, and mark as required

(3) Remove waterseal boot and retaining nut (34) and remove switch (33) and spacer (35).

*b. Reassembly.*

(1) Apply silicone lubricant, specified in paragraph 3–7, to switch (33) mounting area on front panel assembly and to the inside of the waterseal boot.

(2) Install spacer (35) on switch mounting shaft and position switch (33) in mounting hole and secure with waterseal boot and retaining nut (34).

(3) Solder wire to switch terminals, as noted during removal.

(4) Perform step *b* of paragraphs 3–14, 3–13, and 3–12 in this sequence.

3-23. Removal or Replacement of Attenuator 1A1A18-AT1 Boot (fig. 3-7)

*a. Disassembly.* Remove waterseal boots and retaining nuts (36) from attenuator switches.

*b. Reassembly.*

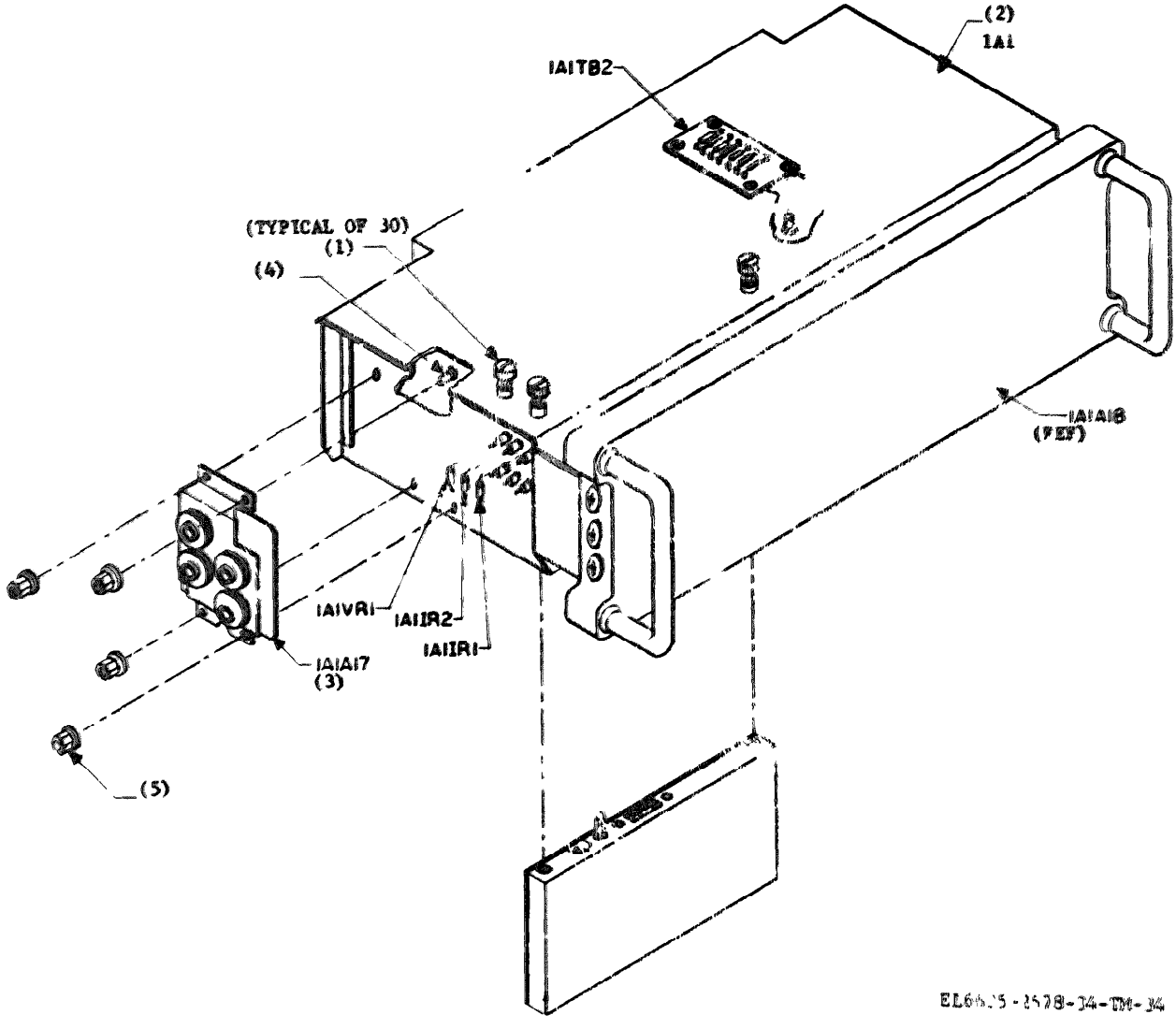
(1) Apply silicone lubricant, specified in paragraph 3–7, to the boot mounting area on the front panel assembly and the inside of the boot.

(2) Position waterseal boot and retaining nut (36) over switch toggle arm and secure by tightening clockwise.

3-24. Removal or Replacement of Plug-In Modules 1A1A1 Through 1A1A15 on Front Panel Module Assembly 1A1 (fig. 3-8).

*a. Disassembly.*

(1) Perform step *a* of paragraphs 3–12 and 3–13.




1 Thumbscrews (30)
2 Front panel module assembly
3 TCXO module
4 Flathead screws (4)
5 Captive washer nut (4)

Figure 3-8. Front panel module assembly 1A1, exploded view.

(2) Loosen two knurled thumbscrews (1) corresponding to the module (1A1A1 through 1A1A15) to be removed.

(3) After loosening, press thumbscrews (1) forward to break module loose from connectors and remove module from opposite side of front panel module assembly 1A1 (2).

*b. Reassembly.*

CAUTION

When replacing modules 1A1A1 through 1A1A15, slide the modules in slowly to avoid possible damage to connector pins.

(1) Slide modules into their appropriate slot and secure by tightening two thumbscrews (1) on opposite side of front panel module assembly.

(2) Perform step *b* of paragraphs 3-11 and 3-12, in this sequence.

3-25. Removal or Replacement of TCXO Module 1A1A16 (fig. 3-1(2)).

*a. Disassembly.*

**(1) Perform step *a* of paragraphs 3–12 and 3–13, in sequence.**

**(2) Unsolder wires and component leads connected to B+, GND and OUT terminals of 1A1A16 (1) and mark wires as required.**

**(3) Remove modules 1A1A2, 1A1A7 and 1A-1A6 (para 3–24) to gain access to two flathead screws (2) on the inside of the front panel module assembly.**

**(4) Remove the two flathead screws (2) and remove module 1A1A16 (1).**

*b. Reassembly.*

**(1) Position module 1A1A16 (1) in place and secure with two flathead screws (2) inserted from inside the front panel module assembly.**

**(2) Replace modules 1A1A2, 1A1A7 and 1A-1A6 (para 3–24).**

**(3) Solder wires and component leads to 1A1A16 terminals (B+, GND and OUT) as noted during removal.**

**(4) Perform step *b* of paragraphs 3–13 and 3–12, in this sequence.**

3-26. Removal or Replacement of Power Supply/Regulator Assembly 1A1A17 (fig. 3-8).

*a. Disassembly.*

**(1) Perform step *a* of paragraphs 3–12 and 3–13.**

**(2) Unsolder wires to 1A1A17 (3) terminals and mark wires as required.**

**(3) Remove modules 1A1A4, 1A1A5, 1A1-A10 and 1A1A11 (para 3–24) to gain access to four flathead screws (4) on the inside of the front panel module assembly.**

**(4) Remove the four flathead screws (4) and the four captive washer nuts (5) securing 1A1A17 (3) to remove 1A1A17.**

*b. Reassembly.*

**(1) Position 1A1A17 (3) in place and secure with four flathead screws (4) and four captive washer nuts (5).**

**(2) Replace modules 1A1A4, 1A1A5, 1A1-A10 and 1A1A11 (para 3–24).**

**(3) Solder wires to 1A1A17 terminals as noted during removal.**

**(4) Perform step *b* of paragraphs 3–13 and 3–12, in this sequence.**

3-27. Removal or Replacement of Connector 1A1P1 on Front Panel Module Assembly (fig. 3-1(2)).

*a. Disassembly.*

**(1) Perform step *a* of paragraphs 3–12 and 3–13.**

**(2) Unsolder wires to connector (3) noting terminal connections, and mark wires as required.**

**(3) Remove two flathead screws (4) and nuts (5) to remove connector (3).**

*b. Reassembly.*

**(1) Position connector (3) in place and secure with two flathead screws (4) and nuts (5).**

**(2) Perform step *b* of paragraphs 3–13 and 3–12, in this sequence.**

3-28. Removal or Replacement of Center Housing Assembly 1A2 Environmental Gasket (fig. 3-9).

*a. Disassembly.*

**(1) Perform step *a* of paragraphs 3–12 and 3–13, in sequence.**

CAUTION

**Sharp tools should not be used when replacing environmental gasket due to the possibility of damaging the gasket during insertion.**

**(2) Loosen and remove environmental gasket (1) from center housing assembly (2).**

*b. Reassembly.*

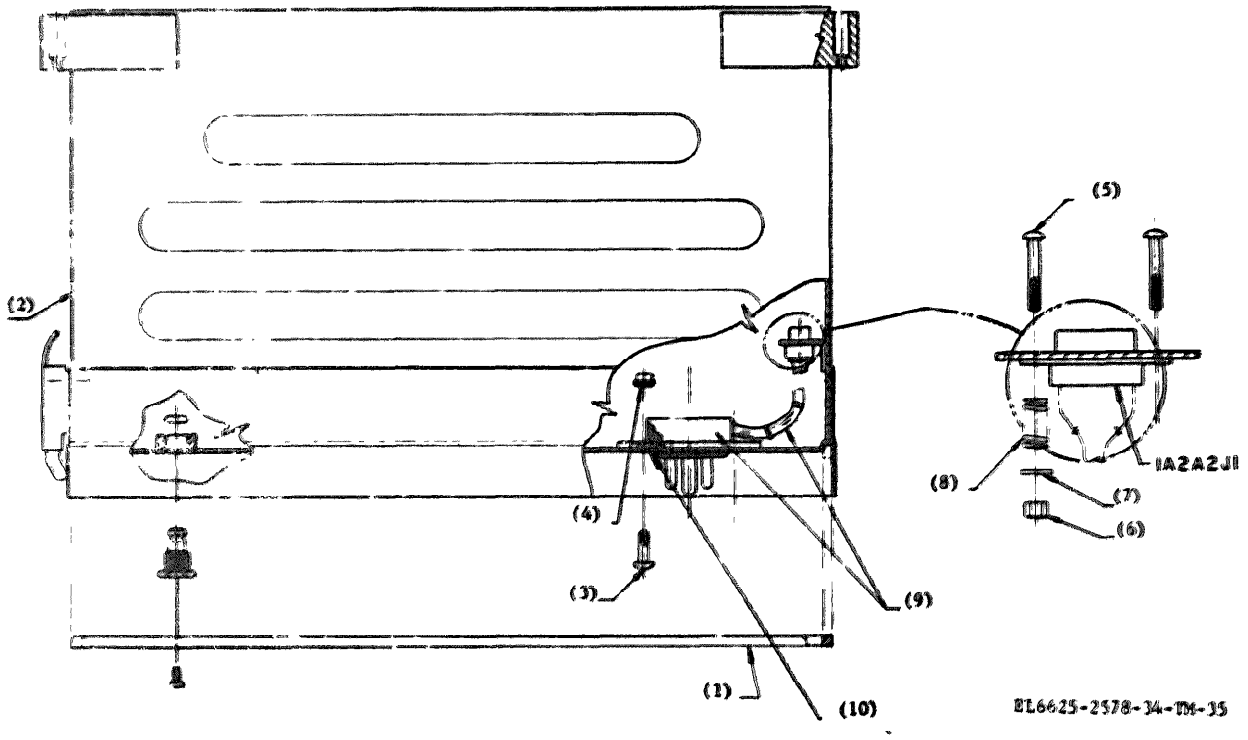
**(1) Apply silicone lubricant, specified in paragraph 3–7, to the new environmental gasket and gasket mounting area.**

**(2) Install new environmental gasket (1) in gasket tray of center housing assembly (2).**

**(3) Perform step *b* of paragraphs 3–13 and 3–12, in this sequence.**

3-29. Removal or Replacement of Connector Assembly 1A2A2 on Center Housing Assembly 1A2 (fig. 3-9)

*a. Disassembly.*




1 Environmental gasket
2 Center housing assembly
3 Panhead screw (6)
4 Nut (6)
5 Panhead screw (2)
6 Nut (2)
7 Flat washer (2)
8 Compression spring (4)
9 Connector assembly 1A2A2
10 O-ring gasket

Figure 3-9. Center housing assembly 1A2, exploded view.

(1) Perform step *a* of paragraphs 3–12 and 3–13, in sequence.

(2) Remove six nuts (4), six panhead screws (3), two nuts (6), two panhead screws (5), two flat washers (7) and four compression springs (8) to take out connector assembly 1A2A2 (9). Remove O-ring gasket (10).

*b. Reassembly.*

CAUTION

Sharp tools should not be used when replacing C-ring gasket due to the possibility of damaging the gasket during replacement.

(1) Apply silicone lubricant, specified in paragraph 3–7, to the new O-ring gasket and gasket mounting area.

(2) Place O-ring gasket (10) in position, put connector assembly 1A2A2 (9) in position and secure with two panhead screws (5), four compression springs (8), two flat washers (7), two nuts (6), six panhead screws (3), and six nuts (4).

(3) Perform step *b* of paragraphs 3–13 and 3–13, in this sequence.

## Section V. TEST SET DIRECT SUPPORT TEST PROCEDURES

### 3-30. General.

*a.* The test procedures described in this section are for use by personnel responsible for direct support maintenance of the test set to determine the acceptability of repaired equipment. These procedures provide specific operational requirements that the equipment must meet before it is returned to service. When a system test procedure does not meet its performance standards, the next higher category of maintenance is required.

CAUTION

**Never adjust any module controls. These controls require specialized test equipment and are adjusted only at depot level.**

*b.* **Comply with all general instructions preceding each test procedure chart. Perform all actions required in the test equipment control settings and test set control settings column of the procedure chart before performing the test procedure steps. Then verify the test procedure results against its performance standard. In addition to these tests, perform the operators test procedures listed in chapter 3 of TM 11–6625–2578–12.**

*c.* **Turn on all test equipment 30 minutes prior to starting any test procedure to allow for warm-up and stabilization. Insure power supplies are set to zero voltage at initial turn-on and then adjusted to specified voltage.**

## 3-31. References

**The following information will be helpful when troubleshooting and/or repairing the test set:**

| | |
|---|---|
| **TM 11-6625-2578-12** | **Operator and Organizational Maintenance Manual for Radio Test Set Group OQ-60/USQ-46.** |
| **Functional block diagram** | **Figure 6-3** |
| **Wiring diagram** | **Figure 6-2** |
| **Schematic diagrams** | **Figures 6-4 through 6-21** |
| **Component locations** | **Section IV** |
| **Front panel controls interlocking diagram.** | **Figure 6-20** |

**NOTE**

**Unless otherwise specified in the test procedures, signal generator output or test set output frequencies have a tolerance of ±5 ppm.**

## 3-32. Guard Band and Sync Pulse Timing Test Procedure

*a. Test Equipment and Materials.*

**(1) Oscilloscope AN/USM-281A**

**(2) RF Monitor R-1617A/USQ-46**

**(3) Power Supply PP-6446A/USQ-46**

*b. Test Connections and Conditions.* **Oscilloscope channel A shall monitor discriminator output of the RF monitor at PIN T on the EXT DISPLAY connector. Connect the equipment as shown in figure 3–10. Waveforms observed during performance of the direct support test procedures are shown in figure 3–11.**

*c. Procedure.* **Perform the steps in chart 3–7.**

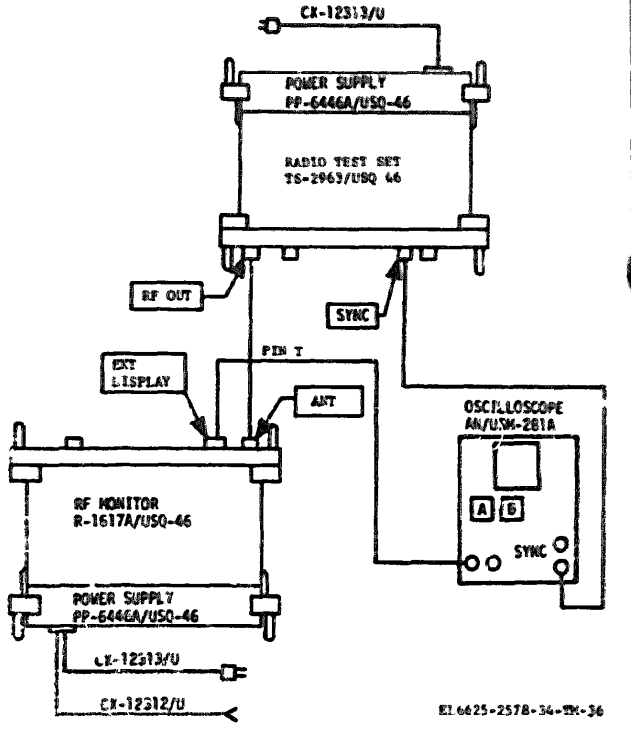



Figure 3-10. Guard band and sync timing test setup.

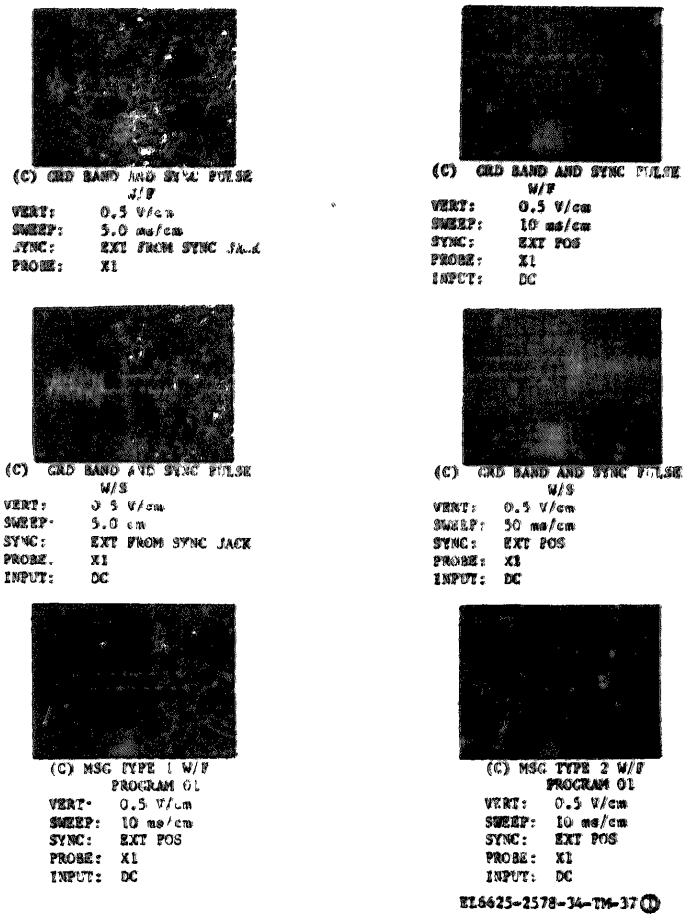



Figure 3-11(1). Direct support test set system waveforms (part 1 of 2).

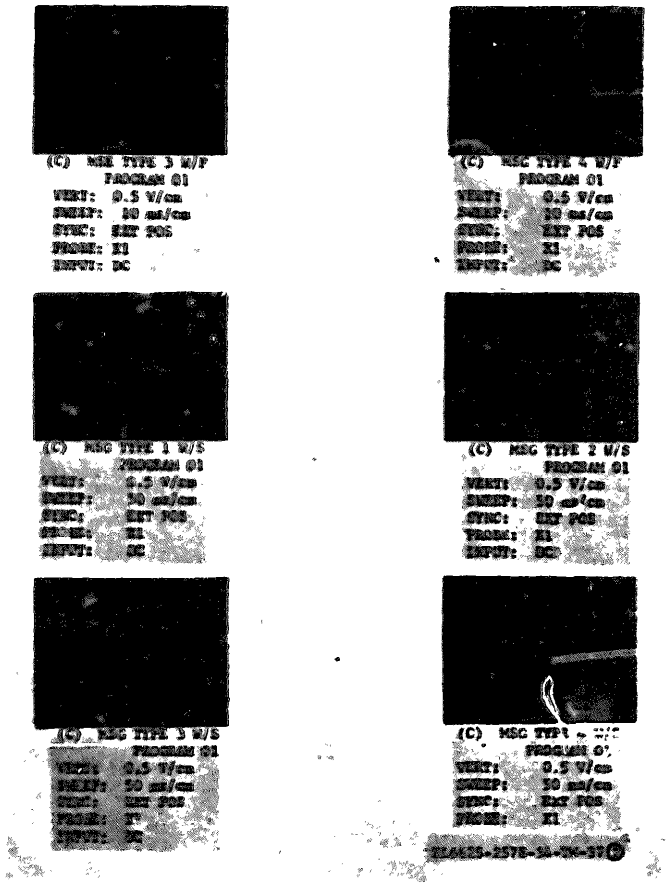



Figure 3-11(2). Direct support test set system waveforms (part 2 of 2).

Chart 3-7. Guard Band and Sync Timing Test Procedure

| Step No. | Test equipment control settings | Test set control settings | Test procedure | Performance standards |
|---|---|---|---|---|
| 1 | *AN/USM-281A*<br>TRIGGER: Ext<br>SWEEP: 5 ms/cm<br>VERT: 2 V/cm<br>*RF MONITOR*<br>CHANNEL: 1045<br>POWER: ON<br>VOLUME: CW<br>SQUELCH: Max. CW<br>DIM: Maximum CW | RF Channel: 1045<br>MODE: REP-A<br>MESSAGE: 1<br>PROGRAM: 01<br>FSK: WP<br>RF OUTPUT ATTEN:<br>−90 dbm (80 db Atten. on switch) | Press START switch | AN/USM-281A must indicate a 5 ± 2 ms noise period from the start of the oscilloscope trace to the beginning of the quieting RF Monitor output, and a 5 ± 0.5 ms quieting period (guard band) prior to the first position transition as shown in waveforms A and B, figure 3-11①. |
| 2 | Same as step 1 except:<br>RF Monitor BIT-RATE to SLOW. | Same as Step 1 except:<br>FSK: W/S | Press START | AN/USM-281A must indicate a 15 ± 5 ms noise period from the start of the oscilloscope trace to the beginning of the quieting RF Monitor output and a 5 ± 0.5 ms quieting period (guard band) prior to the first positive transition as shown in waveforms C and D, figure 3-11①. |

3-33. RF Output Calibration Accuracy Test Procedure

*a. Test Equipment and Materials.* **AN/URM-145.**

*b. Test Connections and Conditions.* **Connect the equipment as shown in figure 3-12.**

*c. Procedure.* **Perform the steps in chart 3-8.**

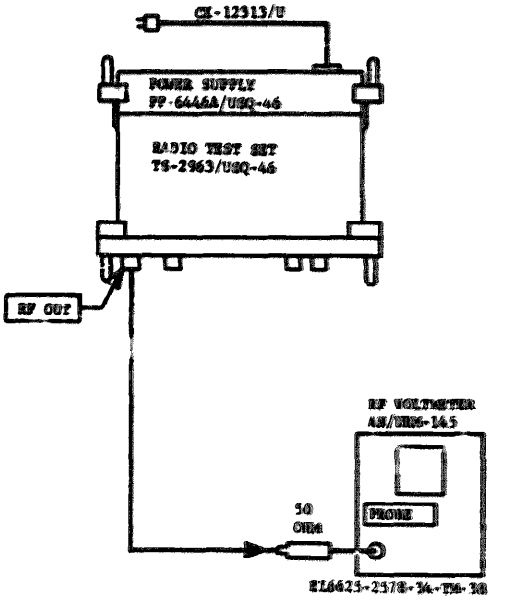



Figure 3-12. RF output calibration accuracy test setup.

Chart 3-8. RF Output Calibration Accuracy Test Procedures

| Step No. | Test equipment control settings | Test set control settings | Test procedure | Performance standards |
|---|---|---|---|---|
| 1 | *AN/URM-145*<br>RANGE: Set for center scale deflection, use test. | RF Channel: 1045<br>METER SW: RF Level<br>MODE: CAL<br>MESSAGE: 1<br>RF OUTPUT ATTEN: ALL OUT | Adjust RF LEVEL SET for convenient reading on AN/URM-145. | Approximately −10 dbm. |
| 2 | Same as step 1 | Same as step 1 | Insert the following OUTPUT ATTEN one at a time.<br>40 db (#1)<br>40 db (#2)<br>20 db<br>10 db<br>5 db<br>3 db<br>2 db<br>1 db | Reading on the AN/URM-145 must be within ±.04 dbm for each attenuation. |
| 3 | Same as step 1 | Same as step 1 except: RF channel number 2401. | Repeat steps 1 and 2 | Same as step 2. |
| 4 | Same as step 1 | Same as step 1 except: RF channel number 2318. | Repeat steps 1 and 2 | Same as step 2. |

3-34. Frequency Coverage and Accuracy Test Procedure

*a. Test Equipment and Materials.* **AN/USM-207 frequency counter.**

*b. Test Connections and Conditions.* **Connect equipment as shown in figure 3-13.**

*c. Procedure.* **Perform the steps in chart 3-9.**

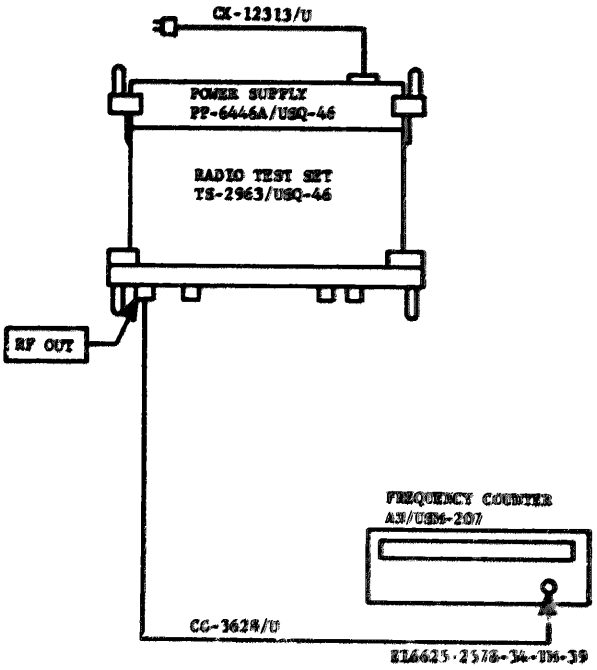



Figure 3-13. Frequency coverage and accuracy test setup.

Chart 3-9. Frequency Coverage and Accuracy Test Procedure

| Step No. | Test equipment control settings | Test set control settings | Test procedure | Performance standards |
|---|---|---|---|---|
| 1 | *AN/USM-207*<br>FUNCTION:<br>FREQUENCY<br>SENSITIVITY: 10 V<br>GATE TIME: As required<br>POWER: TRACK | RF Channel 2400 METER SW: RF Level set (adjust RF level set control for power set line indication on meter).<br>MODE: CAL<br>MESSAGE: 1, 2, or 3<br>RF OUTPUT ATTEN: All to out positions. | Measure output frequency differential on AN/USM-207. | Frequency must be within 5 ppm of channel 2400 (160.125000 MHz). |
| 2 | Same as step 1 | Same as step 1 except: RF CHANNEL number to test channels of chart 3-10. | Same as step 1 | Frequency must be within 5 ppm of channel frequencies listed in chart 3-10. |

Chart 3-10. Test Channel Frequencies

| Channel selected | RF frequency (MHz) |
|---|---|
| 2400 | 160.12500 |
| 2630 | 161.87500 |
| 2699 | 161.99375 |
| 0000 | 162.00000 |
| 0001 | 162.00625 |
| 0109 | 163.68125 |
| 0299 | 163.86875 |
| 0300 | 163.87500 |
| 0427 | 164.66875 |
| 0599 | 165.74375 |
| 0600 | 165.75000 |
| 0736 | 166.60000 |
| 0890 | 167.61875 |
| 0900 | 167.62500 |
| 1045 | 168.53125 |
| 1199 | 169.49375 |
| 1200 | 169.50000 |
| 1354 | 170.46250 |
| 1499 | 171.36875 |
| 1501 | 171.37500 |
| 1699 | 172.39375 |
| 1799 | 173.24375 |
| 1800 | 173.25000 |
| 1972 | 174.32500 |
| 2099 | 175.11875 |
| 2100 | 175.12500 |
| 2218 | 175.86250 |

3-35. Message Program Generation Test

*a. Test Equipment Materials.*

(1) RF Monitor R–1617A/USQ–46.

(2) Power Supply PP–6446A/USQ–46.

(3) RF Indicator ID–1721/USQ–46.

(4) Oscilloscope AN/USM–281A

*b. Test Connections and Conditions.* Connect equipment as shown in figure 3–14.

**NOTE**

If an error is observed on the R–1617A/USQ–46 display during step 1 *a, b, c* or *d,* that step must be repeated three more times to insure that the error was random or that the test step fails to meet the performance standard.

*c. Procedure.* Perform steps of chart 3–11.

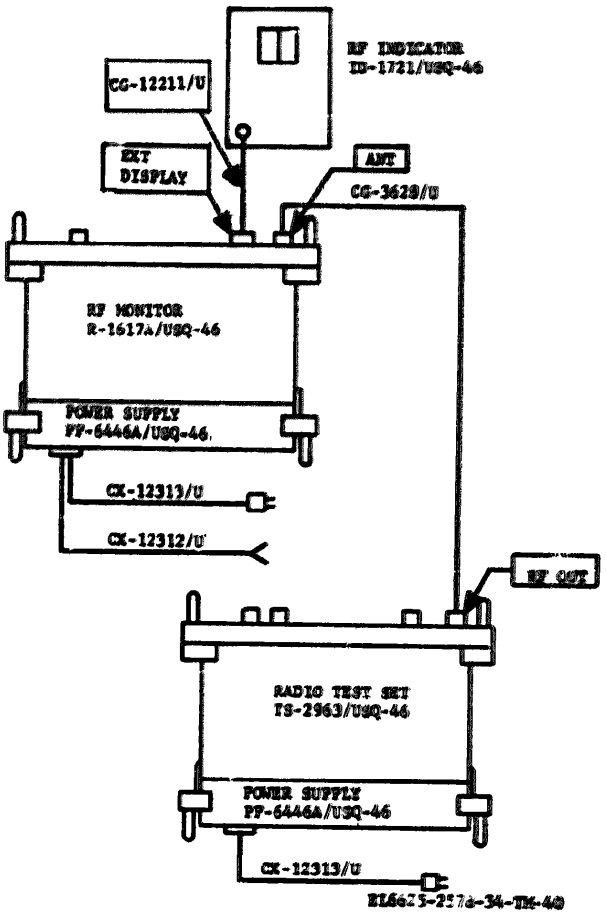



Figure 3-14. Message generation test setup.

Chart 3-11. Message Generation Test Procedure.

| Step No. | Test equipment control settings | Test set control settings | Test procedure | Performance standards |
|---|---|---|---|---|
| 1 | *R-1617A/USQ-46*<br>CHANNEL: 1045<br>PWR: ON<br>VOL: Max CW<br>SQUELCH: Max CCW<br>DIM: Max CW<br>BIT RATE: FAST<br>*AN/USM-281A*<br>TRIGGER: EXT POS<br>COUPLING: DC<br>VERT: 0.5 V/cm<br>SWEEP: 10 ms/cm | METER: RF LEVEL<br>RF ATTEN: 80 dB IN (−90 db at output)<br>RF CHAN: 1045<br>PROGRAM: 01<br>MODE: SEQ-A<br>MESSAGE: 1<br>FSK: W/F | *a.* Press test set START switch | *a.* Lamps 1 through 71 on R-1617A/USQ-46 must light in sequence, and an audible tone must be heard as each lamp lights. Errors (improper sequence or no lamp lit) on the R-1617A/USQ-46 must be less than one error per sequence. (Refer to para 3-35 *b*.) See waveform E, fig. 3-11① for output observed at pin T of R-1617A/USQ-46 external display connector. |
| | | | *b.* Set test set MESSAGE switch to 2 and press START switch. | *b.* Same as step *a* except, ID-1721/USQ-46 message type IIA must remain lit during displays 1 through 71 and the ID-1721/USQ-46 display must show a sequential event count (1 through 63 for R-1617A/USQ-46 displays, 1 through 69 and a 00 for display 71). See waveform F, fig. 3-11① for output observed at pin T of R-1617A/USQ-46 external display connector. The NRT lamp shall indicate a number when the R-1617A/USQ-46 indicates a number as follows:<br>*NRT* — *R-1617A/USQ-46*<br>3 — 38<br>5 — 41<br>6 — 42<br>1 — 45<br>2 — 46<br>4 — 48<br>See waveform A, figure 3-11① output observed at pin T of R-1617A/USQ-46 external display connector. |
| | | | *c.* Set test set MESSAGE switch to 3 and press START switch. | *c.* Same as step *a* except, ID-1721/USQ-46 message type IIB lamp must remain lit during display 1 through 71 and the RT lamp shall indicate a number when the R-1617A/USQ-46 indicates a number as follows:<br>*RT lamp* — *R/1617A/USQ-46*<br>3 — 21<br>5 — 23<br>6 — 24<br>1 — 27<br>2 — 28<br>4 — 31 |

| Step No. | Test equipment control settings | Test set control settings | Test procedure | Performance standards |
|---|---|---|---|---|
| | | | d. Set test set MESSAGE to 4 and MODE switch to REP-M. Manually sequence through all 64 programs with PROGRAM switch. | d. Same as step c except audio tone will be on for 20 ± 2 sec. See waveform B, figure 3-11Ⓑ for output observed at pin T of R-1617A/USQ-46 external display connector. |
| 2 | Same as step 1 except: *AN/USM-281A* SWEEP: 50 ms/cm | Same as step 1 except: FSK: W/S | a. Same as step 1a | a. Same as step 1a except see waveform C, figure 3-11Ⓒ. |
| | | | b. Same as step 1b | b. Same as step 1b except see waveform D, figure 3-11Ⓓ. |
| | | | c. Same as step 1c | c. Same as step 1c except see waveform E, figure 3-11Ⓔ. |
| | | | d. Same as step 1d | d. Same as step 1d except see waveform F, figure 3-11Ⓕ. |

## Section VI. DIREST SUPPORT TROUBLESHOOTING AND REPAIR OF THE POWER SUPPLY PP-6446A/USQ-46

### 3-36. Troubleshooting and Repair

**The following information will be helpful when troubleshooting and/or repairing the power supply:**

| | |
|---|---|
| **TM 11-6625-2578-12** | **Operator and Organizational Maintenance Manual for Test Set Group OQ-60/USQ-46** |
| **Power supply functions** | **Chapter 2** |
| **Functional block diagram** | **Figure 6-3** |
| **Schematic diagram** | **Figure 6-21** |

### 3-37. Resistance Data.

**Charts 3-12 and 3-13 list resistance data to aid in troubleshooting the power supply at the direct support maintenance level. Resistance data was taken on a known good power supply, from connectors J1 and J2 (fig. 3-15①) to chassis ground, with a TS-352B/U multimeter.**

Chart 3-12. J1 Resistance Measurements of the PP-6446A/USQ-46.

| Terminal | Resistance | |
|---|---|---|
| | + Ohms | - Ohms |
| A | Infinite | |
| **B | 250 x 100K | 6.5 x 100 |
| **C | 7 x 100K | 18 x 100 |
| *D | 200 x 100K | - |
| *E | - | - |
| *F | - | - |
| *G | - | - |
| *H | - | - |
| J | Infinite | |
| K | | |
| L | | |
| M | 0 | 0 |

*Terminal not used.
**Measurement at J1-B and J1-C may vary due to condition of electrolytic capacitors in circuit.

Chart 3-13. J2 Resistance Measurements of the PP-6446A/USQ-46.

| Terminal | Resistance | |
|---|---|---|
| | + Ohms | - Ohms |
| A | 0 | 0 |
| *B | 500 x 100K | 2.1 x 10K |
| C | | |
| D | | |
| *E | 300 x 100K | 20 x 100 |

*Measurement at J2-B and J2-E may vary due to condition of electrolytic capacitor in circuit.

### 3-38. Voltage Checks.

*a. General.* **The following voltage checks were made on a known good power supply using a TS-352B/U multimeter A jumper wire was connected between pins C and D to simulate the test set MODE switch. There was no load test set connected to J2.**

*b. AC Input.* **With the power supply ac cable CX-12313/U, connected at J1 to provide 110 vac, 60 Hz input voltage, check dc voltage between J2-A and J2-B and then J2-A and J2-E. Connect negative multimeter probe to J2-A and positive probe to J2-B or J2-E. Voltage between J2-A and J2-B shall be 11.5 to 16.0 vdc. Voltage between J2-A and J2-E should be 22 to 33 vdc.**

### 3-39. Continuity Checks and Input Power Cable.

**Check the power supply ac input power cable for continuity as shown in figure 3-16. Repair or replace cable, if required.**

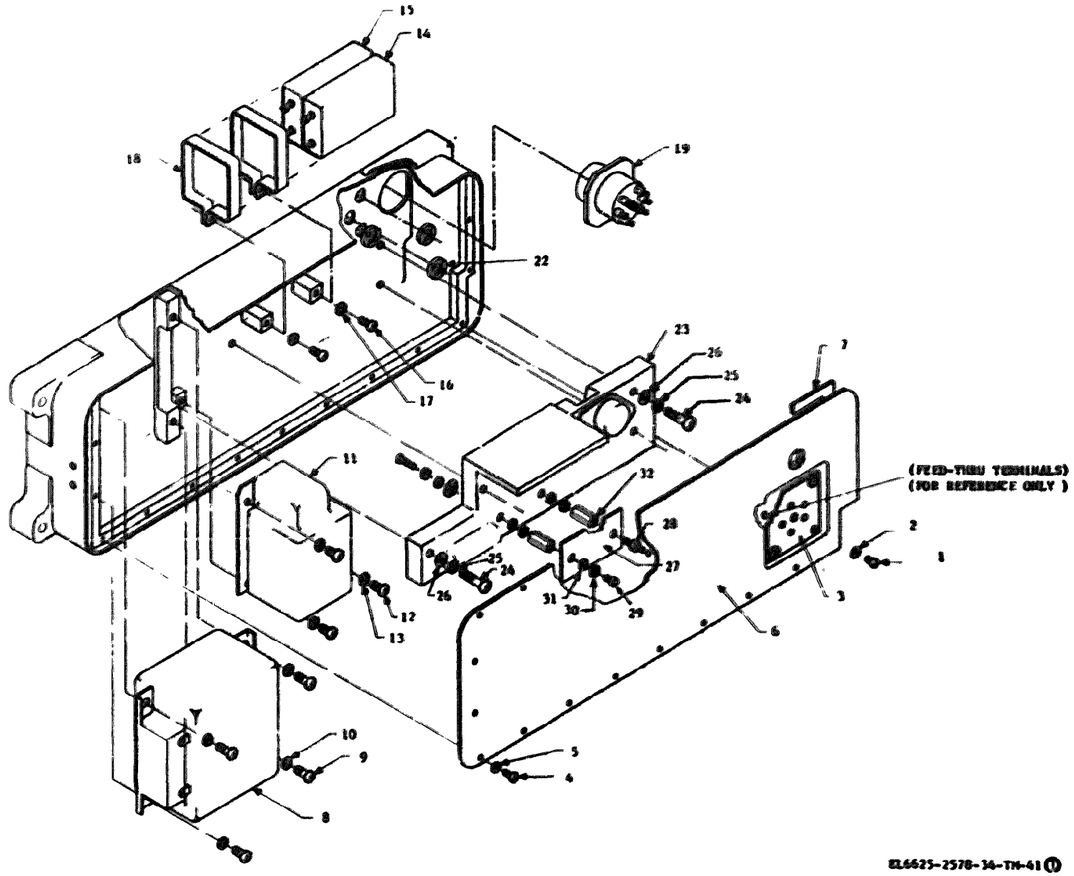
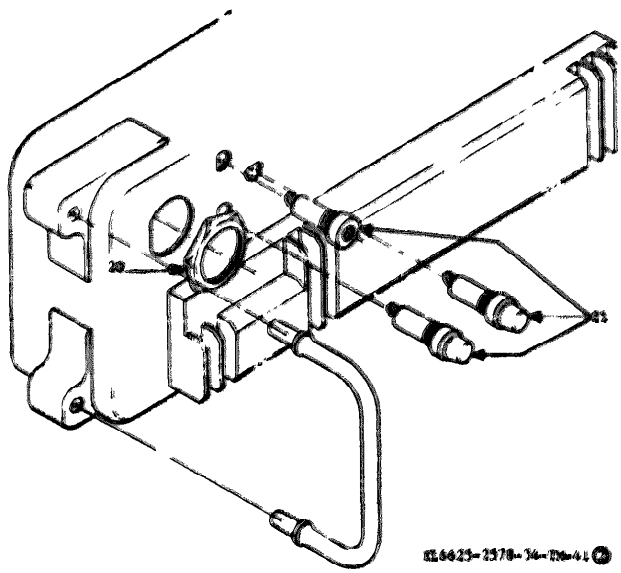



Figure 3-15(1). Power supply PP-6446A/USQ-46. components location (part 1 of 2).

1 Panhead screws (4)
2 Flat washers (4)
3 Connector J2
4 Panhead screws (22)
5 Flat washers (22)
6 Cover plate
7 Environmental gasket
8 Transformer 2T1
9 Panhead screws (4)
10 Flat washers (4)
11 Choke 2L1
12 Flathead screws (3)
13 Flat washers (3)
14 Capacitor 2C1
15 Capacitor 2C2
16 Flathead screws (2)
17 Flat washer (2)
18 Mounting brackets (2)
19 Connector J1
22 Retainer nut
23 Component plate assembly
24 Panhead screws (4)
25 Lockwasher (4)
26 Flat washer (4)
27 Component board
28 Screw terminal
29 Panhead screw
30 Lockwasher
31 Flat washer
32 Standoff (2)

Figure 3-15(1) -- Continued




20 Fuse holders (3) 21 Retainer nuts (3)

Figure 3-15(2). Power Supply PP-6446A/USQ-46. components location (part 2 of 2).

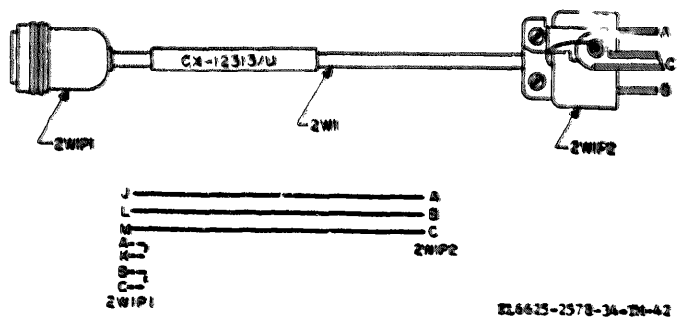



Figure 3-16. Power Supply AC Cable Assembly CX-12313/U.

## Section VII. DIRECT SUPPORT REPAIR PROCEDURES FOR THE POWER SUPPLY PP-6446A/USQ-46.

3-40. Repair Procedures.

*a. General.* When equipment has been turned in for repair, check it for completeness and for condition. Check the preventive maintenance forms to find deficiencies that could not be corrected by organizational maintenance personnel. Check the equipment for tags or notes which may indicate the malfunction of the equipment.

*b. Inspection.* Make a visual inspection to determine the condition of the equipment when it is turned in for repair.

(1) Inspect the cable for broken leads, brittle or damaged insulation, and corrosion.

(2) Inspect all plugs for proper seating, loose or broken leads, and poor solder connections.

(3) Inspect fuse holders for bent contacts, damaged covers and corrosion.

*c. Locating Malfunctions.* Locate malfunctions in accordance with the procedures of section VI, and remove and replace parts in accordance with the procedures of section VIII.

## Section VIII. DIRECT SUPPORT REMOVAL OR REPLACEMENT OF POWER SUPPLY PARTS.

3-41. Removal or Replacement of Connector J 2
(fig 3-15(1) and (2)).

*a. Disassembly.*

(1) Remove four panhead screws (1) and four flat washers (2) to loosen connector J2 (3).

(2) Pull connector J2 (3) out to maximum length allowed by wires connected to rear terminals of J2 (3).

(3) Unsolder wires to connector J2 (3) terminals and remove J2 (3). Note terminal connections and mark wires as required.

*b. Reassembly.*

(1) Solder wires to connector J2 (3) terminals as noted during disassembly.

(2) Position J2 (3) in place and secure with four flat washers (2) and four panhead screws (1).

3-42. Removal or Replacement of Power Supply Gasket
(fig. 3-15(1) and (2)).

*a. Disassembly.*

(1) Remove 22 panhead screws (4) and 22 flat washers (5) securing cover plate (6) and remove cover plate.

CAUTION

Sharp tools should not be used when replacing environmental gasket due to possibility of damaging the gasket during insertion.

(2) Loosen and remove environmental gasket (7) from cover plate (6).

*b. Reassembly.*

(1) Apply adhesive rubber, specified in paragraph 3–7, to one side of the new environmental gasket (7) and gasket area on cover plate (6).

(2) Position treated side of environmental gasket (7) on treated side of cover plate (6).

(3) Apply silicone lubricant, specified in paragraph 3–7, to exposed side of environmental gasket (7) and to power supply housing area that makes contact with gasket.

(4) Position cover plate (6) on power supply housing and secure with 22 flat washers (5) and 22 panhead screws (4).

# CHAPTER 4

# GENERAL SUPPORT MAINTENANCE

## Section I. INTRODUCTION

### 4-1. General

*a.* The additional data and test procedures provided in this chapter are for use by general support maintenance personnel responsible for determining the acceptability of repaired equipment. The test procedures provide specific requirements that a test set must meet after parts have been replaced which require a system accuracy test. These tests are provided in section IV. Additional removal or replacement procedures are provided in section V.

*b.* Test data and procedures for the power supply are provided in section VI. This data provides specific requirements that a power supply must meet after internal parts have been replaced. Additional removal or replacement procedures are provided in section VII

### 4-2. Reference Data

The following information is provided to aid in isolating a faulty module (or replaceable part at general support) in the test set:

| | |
|---|---|
| Voltage and resistance chart | Paragraph 3-5 |
| System waveforms | Paragraph 3-6 |
| Direct support troubleshooting chart | Paragraph 3-11 |
| General support troubleshooting chart | Paragraph 4-4 |
| Functional block diagram | Figure 6-3 |
| Wiring diagram | Figure 6-2 |

## Section II. TOOLS, MATERIALS, AND TEST EQUIPMENT

### 4-3. Tools, Materials, and Test Equipment

All tools, materials and test equipment (in addition to that required for direct support maintenance) required to perform testing procedures in this chapter are listed below.

*a. Tools.* No additional tools are required for general support maintenance.

*b. Materials.* No additional materials are required for general support maintenance.

*c. Test Equipment.* The following test equipment (or equivalent) is required for general support maintenance in addition to the test equipment is listed in paragraph 3-7.

| *Test equipment* | *Common name* |
|---|---|
| Ac Ammeter ME-65A/U | Ac ammeter |
| Dc Ammeter TS-352B/U | Dc ammeter |
| Decade Resistance Box ZM-16B/U | Decade box |
| Digital Voltmeter AN/GSM-64 | Digital voltmeter |
| Variac Autotransformer CN-16/U | Ac power supply |
| Signal Generator AN/URM-70 | Signal generator |
| RMS Voltmeter ME-318/U | RMS voltmeter |
| Signal Generator AN/USM-264 | Signal generator |
| Power Supply PP-6445A/USQ-46 | Power supply |
| Signal Generator SG-299/U | Signal generator |
| Storage oscilloscope HP-1405, 1422, 141S. | Oscilloscope |
| Stoddard attenuators 90513-40 and -60. | Attenuators |
| 100K ohm resistor RC05GF104J | Resistor |

## Section III. GENERAL SUPPORT TROUBLESHOOTING OF TEST SET

### 4-4. Troubleshooting Chart

Troubleshooting chart 4-1 covers symptoms that may be noticed when performing the additional Test Set system tests contained in paragraphs 4-6 through 4-10. If a trouble is noticed during a test procedure, refer to the troubleshooting chart for corrective measures for that trouble.

Chart 4-1. General Support Test Set Troubleshooting Chart

| Item No | Trouble symptom | Probable trouble checks, corrective measures |
|---|---|---|
| 1 | System accuracy incorrect | *a.* Faulty detector-output module 1A1A2 (fig. 3-1). Replace if defective.<br>*b.* Faulty attenuator switch(es). Replace attenuator assembly 1A1A18-AT1 (fig. 3-7). |
| 2 | Meter cannot be set to POWER SET mark. | *a.* Faulty meter 1A1A18-M1 (fig. 3-7). Replace if defective.<br>*b.* Faulty detector-output module 1A1A2 (fig. 3-1). Replace if defective.<br>*c.* Faulty RF mixer/amplifier 1A1A7 (fig. 3-1). Replace if defective.<br>*d.* Faulty VCXO 1A1A1 (fig. 3-1). Replace if defective.<br>*e.* Faulty loop filter/VCO 1A1A3 (fig. 3-1). Replace if defective.<br>*f.* Faulty RF level set potentiometer 1A1A18-R2 (fig. 3-7). Replace if defective. |
| 3 | All channels off frequency | *a.* Faulty VCXO module 1A1A1 (fig. 3-1). Replace if defective.<br>*b.* Faulty RF mixer/amplifier module 1A1A7 (fig. 3-1). Replace if defective.<br>*c.* Faulty programable divider module 1A1A5 (fig. 3-1). Replace if defective.<br>*d.* Faulty TCXO module 1A1A16 (fig. 3-1) Replace if defective.<br>*e.* Faulty power regulator 1A1A17 (fig. 3-1). Replace if defective. |
| 4 | Some channels off frequency | *a.* Faulty synthesizer/mixer module 1A1A4 (fig. 3-1). Replace if defective.<br>*b.* Faulty loop filter/VCO module 1A1A3 (fig. 3-1). Replace if defective.<br>*c.* Faulty programable divider module 1A1A5 (fig. 3-1). Replace if defective.<br>*d.* Faulty reference generator module 1A1A10 (fig. 3-1). Replace if defective.<br>*e.* Faulty RF mixer/amplifier module 1A1A7 (fig. 3-1). Replace if defective.<br>*f.* Faulty channel select switches 1A1A18-S1 through -S4. Replace if defective |
| 5 | Deviation measurement outside of specifications. | *a.* Faulty mode control III module 1A1A11 (fig. 3-1). Replace if defective.<br>*b.* Faulty VCXO module 1A1A1 (fig. 3-1). Replace if defective. |
| 6 | Unable to obtain specified deviation | *a.* Faulty detector-output module 1A1A2 (fig. 3-1). Replace if defective.<br>*b.* Faulty VCXO module 1A1A1 (fig. 3-1). Replace if defective.<br>*c.* Faulty meter 1A1A18-M1 (fig. 3-7). Replace if defective.<br>*d.* Faulty DEV control 1A1A18-R7 (fig. 3-7). Replace if defective. |
| 7 | Excessive drive required to obtain calibrated meter reading. | *a.* Faulty detector-output module 1A1A2 (fig. 3-1). Replace if defective.<br>*b.* Faulty VCXO module 1A1A1 (fig. 3-1). Replace if defective.<br>*c.* Faulty meter 1A1A18-M1 (fig. 3-7). Replace if defective. |
| 8 | Meter deviation reading increased | *a.* Faulty detector-output module 1A1A2 (fig. 3-1). Replace if defective.<br>*b.* Faulty meter 1A1A18-M1 (fig. 3-7). Replace if defective. |

## Section IV. GENERAL SUPPORT SYSTEM TESTS FOR TEST SET

### 4-5. General

*a.* Comply with all general instructions preceding each test procedure chart. Perform all actions required in the test equipment control settings and the test set control settings columns of the chart before performing the test procedure steps. Then verify the test procedure result against its performance standard.

CAUTION

Never adjust any module controls. These controls require specialized test equipment and are adjusted only at the depot level.

*b.* Allow for at least a 30-minute warmup for all test equipment prior to starting any test procedure.

*e.* Waveforms observed while performing general support system tests on the test set are shown in figure 4–1.

*d.* Unless specified in the test procedures, signal generator outputs or test set outputs have a frequency tolerance of ±5 ppm.

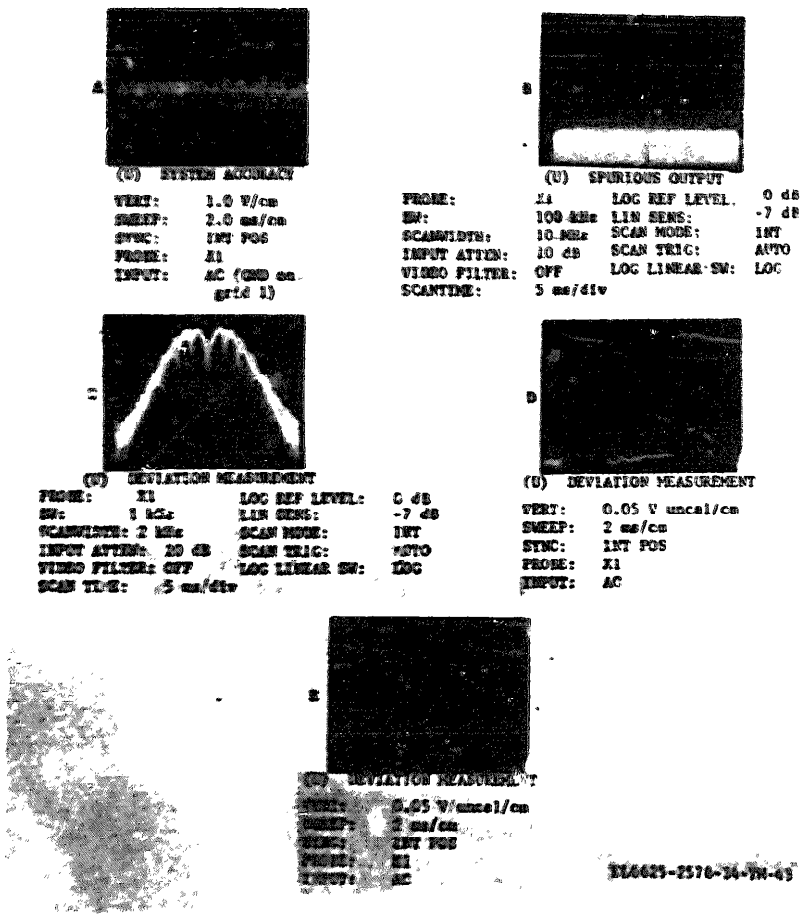



Figure 4-1. General support test set system waveforms.

4-6. RF Output System Accuracy Measurement Test Procedure

*a. Test Equipment and Materials.*

(1) Signal Generator AN/URM–70.

(2) RF Voltmeter AN/URM–145.

(3) Oscilloscope AN/USM–281A.

(4) RMS Voltmeter ME–318/U.

(5) RF Monitor R–1617A/USQ–46.

(6) Stoddard Attenuators 90513–40 and –60.

*b. Test Connections and Conditions.* Connect equipment as shown in figure 4–2.

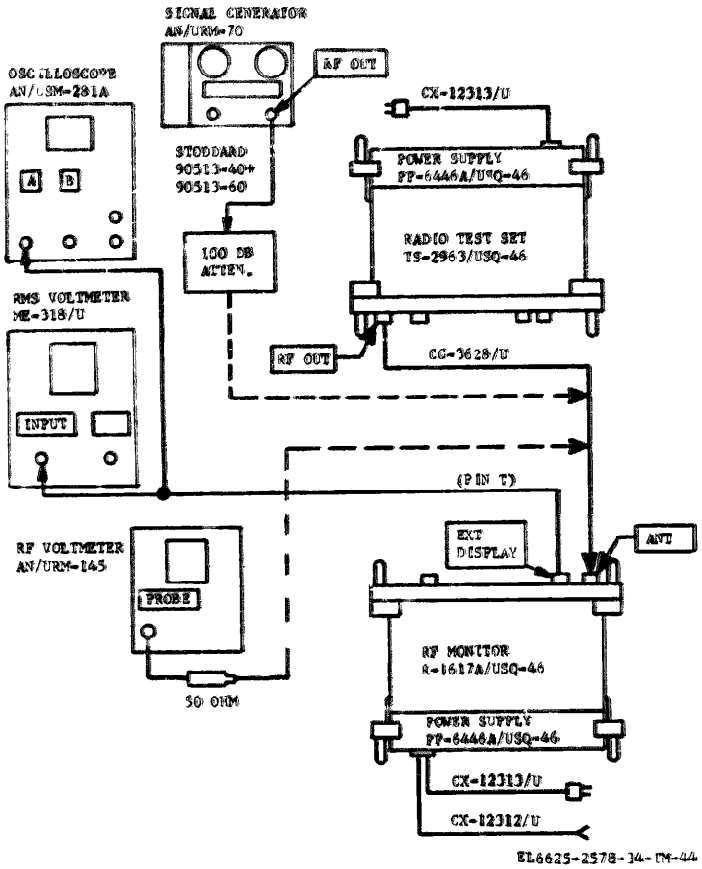



Figure 4-2. RF output system accuracy measurement test setup.

Chart 4-2. RF Output System Accuracy Measurement Test Procedure

| Step No. | Test equipment control settings | Test set control settings | Test procedure | Performance standards |
|---|---|---|---|---|
| 1 | *AN/URM-70*<br>MOD: CW<br>FREQ: 168.531 MHz ± 500 Hz<br>DB OUTPUT: 0 dbm<br>ATTENUATOR: 60 dbm<br>*AN/URM-145*<br>Range: 30 db<br>*AN/USM-281A*<br>TRIGGER: INT. POS.<br>VERT: 1 V/cm<br>SWEEP: 10 ms/cm<br>*ME-318/U*<br>RANGE: 1.0 volt<br>*R-1617A/USQ-46*<br>CHANNEL: 1045<br>PWR: ON<br>VOL: Max CW<br>SQUELCH: Max CW<br>DIM: Max CW<br>BIT-RATE: FAST | RF CHANNEL: 1045<br>RF OUTPUT ATTEN: 40 and 10 IN<br>MODE: CAL<br>MSG: 1, 2, or 3<br>FSK: N/F | *a.* Connect Test Set to R-1617A/USQ-46. De couple AN/USM-281A to pin T of external display connector on R-1617A/USQ-46. Adjust trace on AN/USM-281A. | *a.* Adjust AN/USM-281A vertical control until trace is on centerline of display. |
| | | *b.* Disconnect test set, connect AN/URM-70 through 60 db attenuator pad to R-1617A/USQ-46, and adjust signal generator frequency. | *b.* Adjust frequency until AN/USM-281A trace is on centerline of display. |
| | | *c.* Disconnect AN/URM-70 from attenuator pad and connect to AN/URM-145. Adjust RF output of AN/URM-70. | *c.* Adjust output for a −20 dbm indication. |
| | | *d.* Remove AN/URM-145 and connect AN/URM-70, through 100 db attenuation, to antenna of R-1617A/USQ-46. | *d.* None. |
| | | *e.* Connect ME-318/U to pin T of external display connector and read the rms voltage. | *e.* RMS voltage must be less than 0.2 V rms and greater than 0.05 V rms. Record this reading. |
| | | *f.* Disconnect AN/URM-70 and attenuators from R-1617A/USQ-46. Connect test set to R-1617A/USQ-46. Set test set OUTPUT ATTEN to 40, 40, 20, 5, 3 and 2 IN. Adjust RF LEVEL SET for a POWER SET indication on test set meter. Read output on ME-318/U. | *f.* The same rms voltage ±5% as achieved in step *e* must be indicated on ME-318/U. |
| | | *g.* Disconnect test set from R-1617A/USQ-46, connect test set to AN/URM-145. Set OUTPUT ATTEN switches to OUT. Observe output of test set on AN/URM-145. | *g.* Output indication shall be −10 ±1.5 dbm. System accuracy is difference in db from −10 dbm. |
| | | *h.* Disconnect test set from AN/URM-145 and connect it to R-1617A/USQ-46. | *h.* None. |
| | | *i.* Set test set and R-1617A/USQ-46 to channel 2213 Adjust test set to POWER SET mark. Set OUTPUT ATTEN 40, 40, 20 and 20 | *i.* Record this reading (see waveform A, figure 4-1). |

| Step No. | Test equipment control settings | Test set control settings | Test procedure | Performance standards |
|---|---|---|---|---|
| | | | switches to IN (−120 dbm output). Observe reading on ME-318/U. | |
| | | | *j.* Disconnect ME-318/U and connect AN/USM-281A to pin T of external display connector. | *j.* Adjust AN/USM-281A until trace is on the centerline of display. |
| | | | *k.* Set AN/URM-70 to 175.852 MHz ±500 Hz at −10 dbm output. Connect AN/URM-70 through 100 db attenuator pad to antenna of R-1617A/USQ-46. Adjust frequency output of AN/URM-70. | *k.* Adjust frequency until trace is on centerline of display. |
| | | | *l.* Adjust the RF output of the AN/URM-70. | *l.* Adjust output to give same reading achieved in step *i.* |
| | | | *m.* Remove AN/URM-70 and 100 db attenuators from R-1617A/USQ-46. Connect AN/URM-70 direct to AN/URM-145 and observe reading. | *m.* Reading should be −20 ±1.5 dbm. System accuracy is difference in db from −20 dbm. |
| | | | *n.* Repeat steps *k* through *m* above for channel 2401 with AN/URM-70 set to 160.731 MHz ±500 Hz. | *n.* Same as steps *k* through *m* above. |

4-7. Spurious Output Test Procedure

*a. Test Equipment and Materials.* Spectrum Analyzer AN/UPM-84.

*b. Test Connections and Conditions.* Connect the equipment as shown in figure 4-3. Set the test set to POWER SET on each channel listed in step *a*, and adjust the AN/UMP-84 for a zero reference level.

*c. Procedure.* Perform steps in chart 4-3.

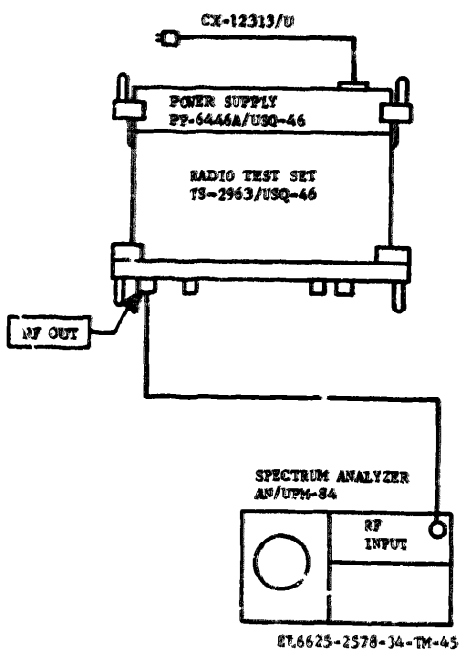



Figure 4-3. Spurious output test setup.

Chart 4-3. Spurious Output Test Procedure

| Step No. | Test equipment control settings | Test set control settings | Test procedure | Performance standards |
|---|---|---|---|---|
| 1 | *AN/UPM-84*<br>**FREQUENCY**: See procedure.<br>**SCANWIDTH**: 5 MHz<br>**BANDWIDTH**: 100 MHz<br>**SCAN TRIGGER**: Auto<br>**LOG/LINEAR**: Log<br>**LOG REFERENCE**: 0 db<br>**INPUT ATTEN**: 20 db<br>**SCANTIME**: 5 ms/div | **RF CHANNEL**: 2400<br>**MODE**: CAL<br>**MSG**: Any<br>**FSK**: W/F<br>**RF OUTPUT ATTEN**: 0 | **Check the output of each channel harmonics listed below.**<br>*Channel* — *(Hz) Frequency*<br>2400 — 160125000<br>2630 — 161875000<br>2699 — 161993750<br>0000 — 162000000<br>0001 — 162006250<br>0109 — 162681250<br>0295 — 163868250<br>0300 — 163875000<br>0427 — 164668750<br>0599 — 165743750<br>0600 — 165750000<br>0736 — 166600000<br>0899 — 167618750<br>0900 — 167625000<br>1045 — 168531250<br>1199 — 169493750<br>1200 — 169500000<br>1354 — 170462500<br>1499 — 171368750<br>1500 — 171375000<br>1663 — 172393750<br>1799 — 173243750<br>1800 — 173250000<br>1972 — 174324000<br>2099 — 175118750<br>2100 — 175125000<br>2218 — 175862500 | **All spurious responses shall be −40 dbm or more down from the carrier. (B, Figure 4-1 for channel 1045 is a typical waveform.)** |

4-8. Deviation Measurement Test

*a. Test Equipment and Materials.*

(1) Signal Generator AN/USM-264.

(2) Frequency Counter AN/USM-207.

(3) Spectrum Analyzer AN/UPM-84.

(4) Signal Generator AN/URM-70.

(5) Power Supply PP-3940A/G.

(6) RF Monitor R-1617A/USQ-46.

(7) Power Supply PP-6446A/USQ-46.

(8) Signal Generator SG-299/U.

(9) 100 K ohm resistor RC05GF104J (2 required).

*b. Test Connectors and Conditions.* Two test setups (figs. 4-4 and 4-5) and four tests are required. Wide deviation test equipment calibration is test 1, wide deviation measurement is test 2, narrow deviation test equipment calibration is test 3, and narrow deviation measurement is test 4. Connect the equipment as noted in the individual test procedures.

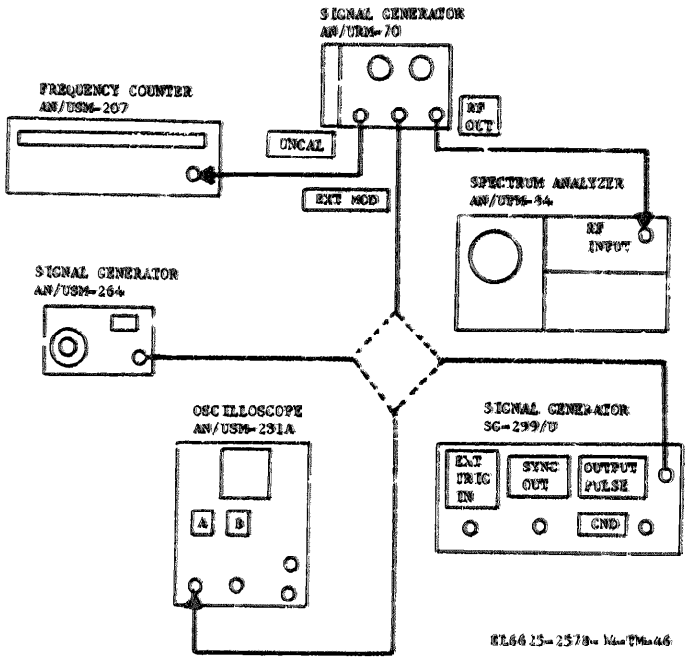



Figure 4-4. Deviation test equipment calibration test setup.

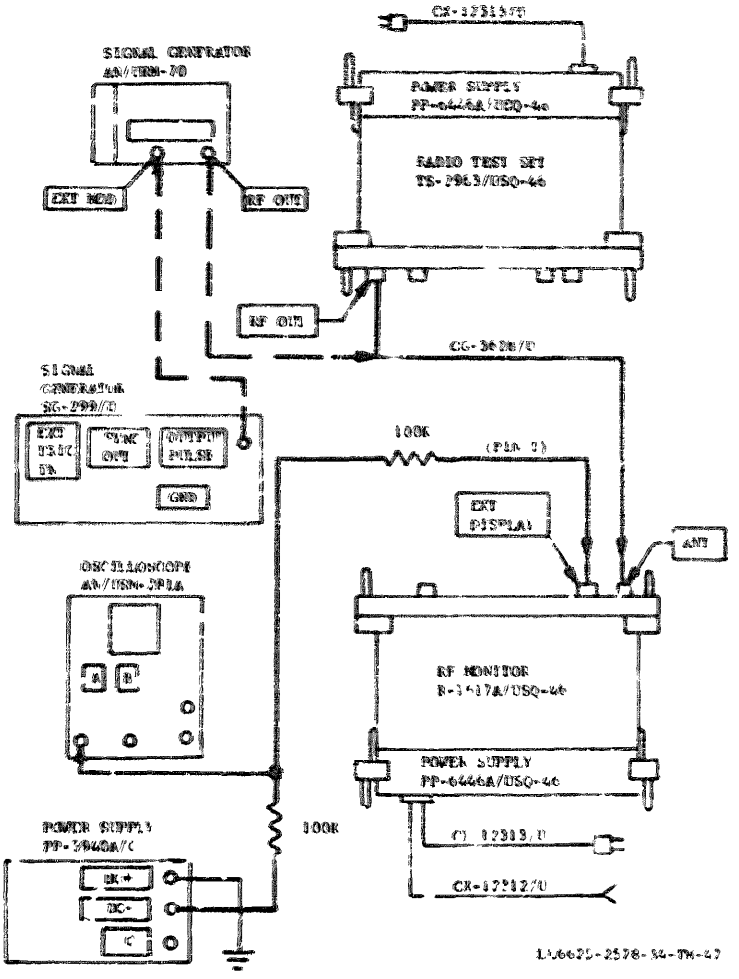



Figure 4-5. Deviation measurement test setup.

Chart 4-4. Deviation Measurement Test Procedure

| Step No. | Test equipment control setting | Test set control settings | Test procedure | Performance standards |
|---|---|---|---|---|
| 1 | *AN/URM-70*<br>FREQUENCY:<br>168.531 MHz ±250 Hz<br>OUTPUT: −50 dbm<br>MODULATION: EXT<br>*AN/USM-264*<br>FREQUENCY:<br>1.250 kHz ± 5 Hz<br>OUTPUT: 0<br>*AN/USM-207*<br>FUNCTION: FREQUENCY<br>SENSITIVITY: 10 V<br>GATE TIME: As required.<br>PWR: TRACK<br>*AN/UPM-84*<br>BANDWIDTH: 30 kHz<br>SCANWIDTH: 1 MHz<br>SCAN TIME: 5 ms<br>ATTENUATION: 0<br>LOG REF SCALE: −30<br>LIN SENS: As required.<br>*AN/USM-281A*<br>TRIG: INT<br>VERT: 2 V/cm<br>SWEEP: 1 ms/cm<br>COUPLING: dc<br>*SG-299/U*<br>FREQUENCY: 75 ±1 Hz<br>OUTPUT: As required. | | *Wide Deviation Calibration*<br>*a.* Connect test equipment as shown in figure 4-4.<br>*b.* With AN/USM-264 disconnected, adjust the frequency of the AN/URM-70 and the AN/URM-84.<br>*c.* Connect AN/USM-264 to EXT modulation input of AN/URM-70.<br>*d.* Adjust AN/UPM-84 frequency coverage.<br>*e.* Increase the output level of AN/USM-264.<br>*f.* Disconnect AN/USM-264 from the AN/URM-70 and connect it to AN/USM-281A.<br>*g.* Disconnect AN/USM-264 from AN/USM-281A and connect the SG-299/U to the AN/USM-281A. Adjust the output level of the SG-299/U. | *a.* None.<br>*b.* Adjust AN/URM-70 to 168.531 MHz ± 250 Hz and adjust AN/UPM-84 to display this frequency on the centerline of the grid.<br>*c.* None.<br>*d.* Alternately decrease AN/UPM-84 bandwidth, scan width and scan time controls until the bandwith control reads .3 kHz, the scan width control reads 2 kHz and the scan time control reads 20 msec while keeping the display centered on the AN/UPM-84 grid.<br>*e.* Increase the output level until the first carrier null is observed on the AN/UPM-84. (Refer to waveform *e*, figure 4-1).<br>*f.* Measure the peak to peak output level of the AN/USM-264 on the AN/USM-281A and note this level.<br>*g.* Adjust the output level of the SG-299/U to a peak-to-peak amplitude equal to that of the AN/USM-264. This level must remain constant throughout the wide deviation portion of the test. |
| 2 | *AN/URM-70*<br>Same as in step 1.<br>*AN/USM-281A*<br>Same as in step 1 except SWEEP is 2 msec.<br>*SG-299/U*<br>Same as in step *1g*. | MODE: CAL ..... | *Wide Deviation Measurement*<br>*a.* Connect test equipment as shown in figure 4-5.<br>*b.* Ground input of AN/USM-281A and adjust trace.<br>*c.* Adjust PP-3940A/G<br>*d.* Disconnect the radio test set from | *a.* None.<br>*b.* Adjust trace to center of screen. Unground AN/USM-281A input.<br>*c.* Adjust output voltage to recenter the AN/USM-281A trace.<br>*d.* Adjust fine tuning to recenter the AN/ |

| Step No. | Test equipment control settings | Test set control settings | Test procedure | Performance standards |
|---|---|---|---|---|
| | *PP–3940A/G*<br>VOLTAGE: As required.<br>*R–1617A/USQ–46*<br>PWR: ON<br>DIM: CW<br>AUDIO: CW<br>SQUELCH: CW<br>CHANNEL: 1045 | FSK: W/F<br>MESSAGE TYPE: 1, 2 or 3.<br>MESSAGE: 01<br>RF LEVEL: PWR SET.<br>CHANNEL: 1045 | the R–1617A/USQ–46 and connect AN/URM–70 to the R–1617A/USQ–46. Adjust fine tuning control of the AN/URM–70.<br>*e.* Connect SG–299/U to EXT MOD input of AN/URM–70 and adjust AN/USM–281A.<br><br>*f.* Disconnect the AN/URM–70 from R–1617A/USQ–46 and connect the radio test set to the R–1617A/USQ–46. Set radio test set MESSAGE TYPE switch to 4. | USM–281A trace.<br><br>*e.* Adjust vertical gain to give a 6 cm peak to amplitude square wave, symmetrical about the centerline. (Refer to waveform D figure 4–1). Recenter the display as necessary with vertical position control of the AN/USM–281A.<br><br>*f.* AN/USM–281A should display a 75 ± 1 Hz square wave, 6 ±0.3 cm about the centerline, (refer to waveform E figure 4–1). The deviation meter of the radio test set should indicate approximately 3. |
| 3 | | | *Narrow Deviation Calibration* | |
| | Same as step 1 except:<br>*AN/USM–264*<br>FREQUENCY: 625 ± 5 Hz.<br>*AN/USM–281A*<br>VERTICAL: 1 V/div. | Same as step 2 | Repeat step 1*a* through *g* | Same as step 1*a* through *g* except, the level of step 1*g* must remain constant throughout the narrow deviation portion of the test. |
| 4 | | | *Narrow Deviation Measurement* | |
| | *AN/URM–70*<br>Same as step 1.<br>*AN/USM–281A*<br>Same as step 3 except:<br>SWEEP: 2 ms/cm.<br>*SG–299/U*<br>Same as in 1*g*.<br>*PP–3940A/G*<br>VOLTAGE: As required.<br>*R–1617A/USQ–46*<br>Same as step 2. | Same as step 2 except:<br>FSK: N/F | *a.* Repeat steps 2*a* through *f*<br><br>*b.* Ground the input of the AN/USM–281A. | *a.* Same as step 2*a* through *f* except, the radio test set deviation of step 2*f* should indicate approximately 1.5.<br><br>*b.* AN/USM–281A trace must be within 0.4 cm of centerline. |

4-9. Current Drain Test

*a. Test Equipment and Materials.*

(1) Multimeter TS–352B/U.

(2) Ac Ammeter ME–65A/U.

(3) Auto Transformer CN–16/U.

*b. Test Connections and Conditions.* C the equipment as shown in figure 4–6.

*c. Procedure.* Perform steps of chart 4–5.

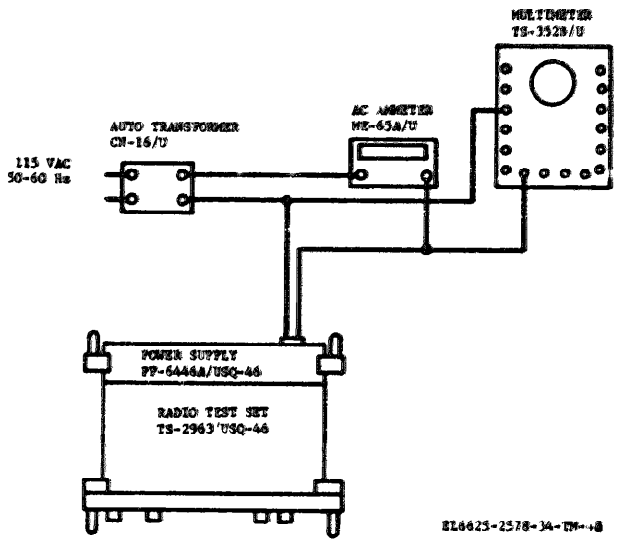



Figure 4-6. Current drain test setup.

Chart 4-5. Current Drain Test Procedure

| Step No. | Test equipment control settings | Test set control settings | Test procedure | | Performance standards |
|---|---|---|---|---|---|
| 1 | *CN-16/U*<br>**VOLTAGE: 132 vac**<br>*TS-352B/U*<br>**FUNCTION: ac volts**<br>**RANGE: 250 vac**<br>*ME-65A/U*<br>**RANGE: 250 ma** | **Test Set controls can be in any position except MODE to CAL.** | **Measure and note current drain** | ... | **Current drain shall not be greater than 250 ma.** |

4-10. Keying Rate Measurement Test Procedure

*a. Test Equipment and Material.*

(1) Oscilloscope, HP 1405, 1422, 141S.

(2) Frequency Counter AN/USM-207.

*b. Test Connections and Conditions.* Connect equipment as shown in figure 4-7, with center housing assembly separated (para 3-13) and extender cable connected (para 3-7).

*c. Procedure.* Perform the steps in chart 4-6.

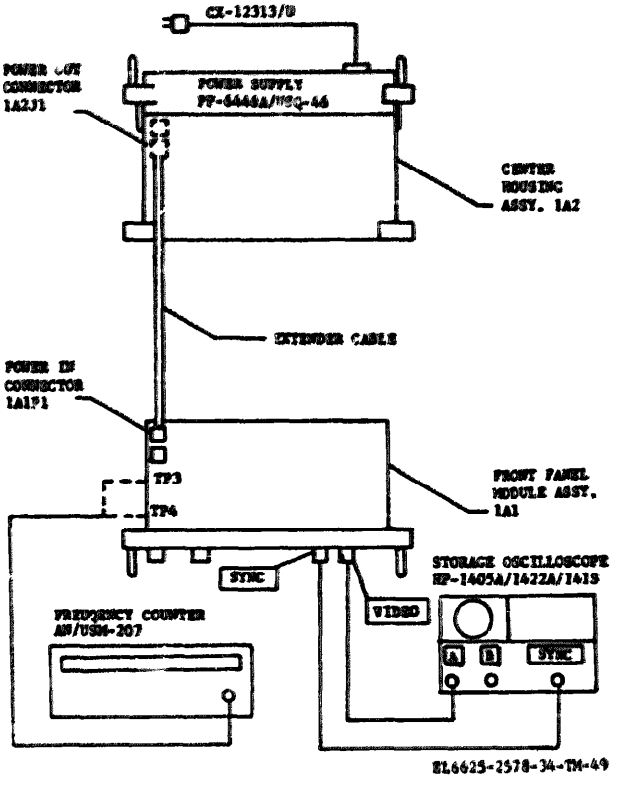



Figure 4-7. Keying rate measurement test setup.

Chart 4-6. Keying Rate Measurement Test Procedure

| Step No. | Test equipment control settings | Test set control settings | Test procedure | Performance standards |
|---|---|---|---|---|
| 1 | *HP–1405, 1422, 141S*<br>TRIGGER: EXT<br>SWEEP: 1 ms/cm<br>VERT: 1 v/cm<br>Note: Use DELAYED SWEEP as necessary. | MODE: REP–A<br>PROGRAM: 01<br>MESSAGE: 1<br>FSK: any position (see Procedure). | Press START switch and setup video on the HP–141S. Choosing FSK "0" bits at start of data word, the display should be adjusted to indicate time between FSK transitions. | Transition rate shall be approximately 1.67 msec in FSK switch positions N/F and W/F (300 Hz data rate). Transition rate shall be approximately 6.66 msec in FSK switch position N/S and W/S (75 Hz data rate). |
| 2 | *AN/USM–207*<br>FUNCTION: FREQUENCY<br>SENSITIVITY: 10 v<br>POWER: TRACK<br>GATE TIME: As required. | Same as step 1 | Connect AN/USM–207 to 1A1A11–TP–3 (Mode Control III). | Frequency must be 75 Hz ±3%. (Waveform is same as A fig. 3–4Ⓣ). |
| 3 | Same as step 2. | Same as step 1 | Connect AN/USM–207 to 1A1A11–TP4 (Mode Control III). | Frequency must be 300 Hz ±3%. (Same as waveform B fig. 3–4Ⓣ.) |

## Section V. GENERAL SUPPORT REMOVAL AND REPLACEMENT OF TEST SET COMPONENTS

### 4-11. General

This section provides detailed removal and replacement instructions for test set components that are replaceable at the general support level. When it is necessary to replace a component which is accessible without disassembling the entire equipment, perform only those steps necessary to reach that component.

### 4-12. Removal or Replacement of Attenuator 1A1A18 AT1 (fig. 3-7).

*a. Disassembly.*

(1) Perform step *a* of paragraphs 3–12, 3–13, and 3–14 in sequence.

(2) Disconnect input and output cable connectors at rear of attenuator (23).

(3) Perform step *a* of paragraph 3–23 to remove waterseal boots on the switches of attenuator (23); then pull the attenuator out from back side of front panel assembly (1).

*b. Reassembly.*

(1) Place AT1 in position from back side of front panel assembly 1A1A18 (1) and push forward so that the attenuator switches protrude through the front panel assembly (1).

(2) Secure attenuator (23) by performing step *b* of paragraph 3–23.

(3) Connect input and output cable connectors at rear of attenuator (23).

(4) Perform step *b* of paragraphs 3–14, 3–13, and 3–12 in sequence.

### 4-13. Removal or Replacement of Meter 1A1A18-M1 (fig. 3-7).

*a. Disassembly.*

(1) Perform step *a* of paragraphs 3–12, 3–13, and 3–14 in sequence.

(2) Unsolder wires at terminals of meter (37), noting terminal connections, and mark wires as required.

(3) Remove four panhead screws (38) to remove meter (37) from the back side of front panel assembly (1).

*b. Reassembly.*

(1) Apply silicone lubricant, as specified in paragraph 3–7, to mounting area of meter (37) and front panel assembly (1).

(2) Position meter (37) in place and secure with four panhead screws (38).

(3) Solder wires to meter (37) terminals as noted during disassembly.

(4) Perform step *b* of paragraphs 3–14, 3–13, and 3–12 in this sequence.

### 4-14. Removal or Replacement of Variable Resistors 1A1A18-R1 or 1A1A18-R2 (fig. 3-7).

*a. Disassembly.*

(1) Perform step *a* of paragraphs 3–12, 3–13, and 3–14 in sequence.

(2) Unsolder wires to resistors R1 (39) or R2 (40), noting terminal connections, and mark wires as required.

(3) Perform step *a* of paragraph 3–16 to remove resistor (39 or 40) knobs (5).

(4) Remove nut (6) and lockwasher (7) to remove resistor (39 or 40) by pulling it from the rear of the front panel assembly (1). Items (6) and (7) are supplied with each replacement resistor and therefore need not be saved during removal.

*b. Reassembly.*

(1) Apply silicone lubricant, as specified in paragraph 3–7, to mounting area of resistor (39 or 40) and front panel assembly (1).

(2) Position resistor (39 or 40) in place and secure it with lock washer (7) and nut (6).

(3) Perform step *b* of paragraph 3–16, replace knob (5).

(4) Solder wires to resistor (39 or 40) as noted during disassembly.

(5) Perform step *b* of paragraphs 3–14, 3–13, and 3–12 in this sequence.

## Section VI. GENERAL SUPPORT TROUBLESHOOTING OF POWER SUPPLY

### 4-15. General

**Troubleshooting of the power supply at the general support maintenance level consists of performing voltage and resistance checks (in addition to those in para 3–37 and 3–38) and system tests. Troubleshooting chart 4–7 is provided which lists symptoms that may be noted when performing the system tests (para 4–18 through 4–21). If a trouble is noted during a test, refer to the troubleshooting chart for corrective measures for that trouble.**

### 4-16. Reference Data

**Refer to figure 3–15① and ② and figure 4–8 for power supply components locations and paragraphs 4–25 through 4–30 for component removal or replacement instructions. Refer to chapter 2, for functioning of the power supply and figure 6–21 for the power supply schematic diagram.**

### 4-17. Voltage and Resistance Chart

**Voltage and resistance measurements of the power supply transistors are provided in chart 4–8. This chart and the resistance charts of paragraph 3–37 are provided to aid general support maintenance personnel in detailed troubleshooting of the power supply. The equipment was connected as shown in figure 4–9.**

Chart 4-7 General Support Power Supply Troubleshooting Chart

| Item No. | Trouble symptom | Probable trouble checks, corrective measures |
|---|---|---|
| 1 | No regulated or unregulated output for either ac or dc inputs. | Check for defective FL1, FL2, R1, R4, Q1, Q2, Q3, VR1 or C6. Replace defective component. |
| 2 | No regulated output, but unregulated output is OK. | Check for defective component in 12 V regulator circuit. Replace defective component. |
| 3 | Regulated output indicates instability. | Check for defective VR2 and components in the 12 V or 27 V regulator circuits. Replace defective component. |
| 4 | Excessive current drain | Check for defective C1, C2, C3, CR1, or T1 and components in the 12 or 27 V regulator circuits. Replace defective component. |
| 5 | Regulated output not within limits in ac mode only. | Check for defective C1, C2 and CR1. Replace defective component. |
| 6 | Excessive ripple on output of 12 and 27 V regulators in ac mode. | Check for defective C1, C2 and L1. Replace defective component. |

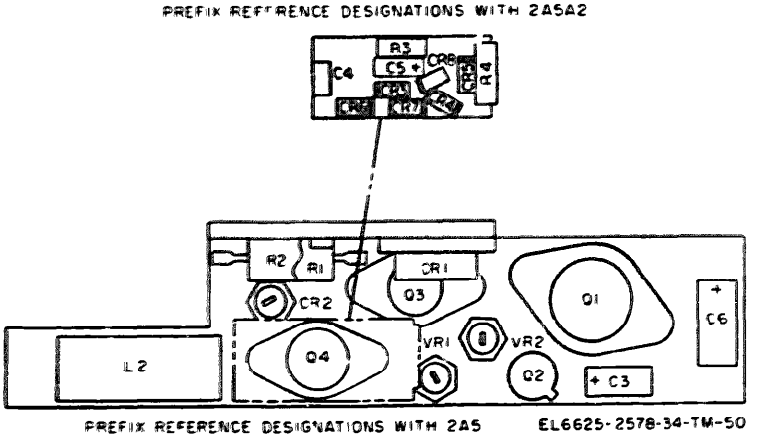



Figure 4-8. Component plate and component board assembly component location.

*a. Resistance.* **All measurements were taken with respect to chassis ground using a TS–352B/U multimeter. No power was applied.**

***b. Voltage.*** **All measurements were taken with respect to chassis ground using a Digital Voltmeter AN/GSM–64. Input voltage to the power supply was nominal 115 vac, 50–60 Hz.**

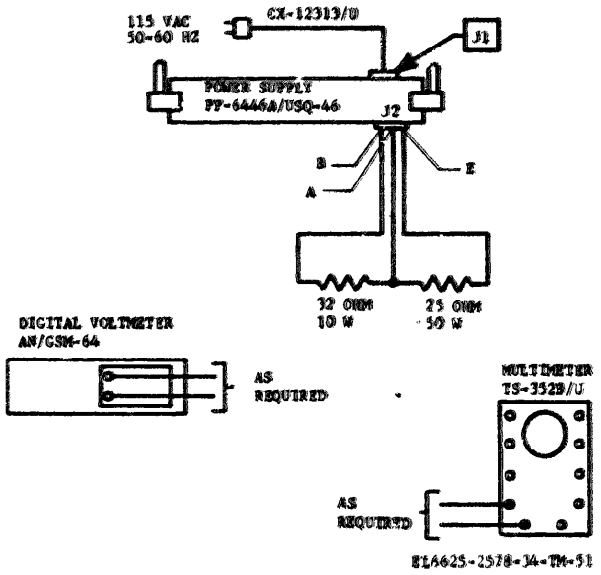



Figure 4-9. Power supply troubleshooting test setup.

Chart 4-8. Power Supply Voltage and Resistance Measurements.

| Transistor | Collector | | | Base | | | Emitter | | |
|---|---|---|---|---|---|---|---|---|---|
| | DC Volt | Ohms | Range | DC Volt | Ohms | Range | DC Volt | Ohms | Range |
| 2N3442 Q1 | 26.40 | 6.80 | X100 | 26.27 | * | | 25.60 | 2500 | X100 |
| 2N4239 Q2 | 25.73 | 2550 | X100 | 26.19 | 820 | X100 | 25.60 | 2509 | X100 |
| 2N3741 Q3 | 26.37 | * | | 25.73 | 2550 | X100 | 26.40 | 680 | X100 |
| 2N3767 Q4 | 25.50 | 240 | X100 | 14.91 | 285 | X100 | 14.19 | 28.5k | X10k |

*No ohmeter reading due to capacitive circuit.

Section VII. GENERAL SUPPORT POWER SUPPLY TEST PROCEDURES

4-18. Dc Mode Voltage Regulation Test Procedure

*a. Test Equipment and Materials.*

(1) Oscilloscope AN/USM-281A.
(2) Digital Voltmeter AN/GSM-64.
(3) DC Ammeter TS-352B/U (2 required).
(4) Decade Resistance Box ZM-16B/U (2 required).
(5) Power Supply PP-3940A/G.

*b. Test Connections and conditions.* Connect equipment as shown in figure 4-10. The input dc ammeter (TS-352B/U) is set for 5a but is not required for this test.

*c. Procedure.* Perform the steps of chart 4-9.

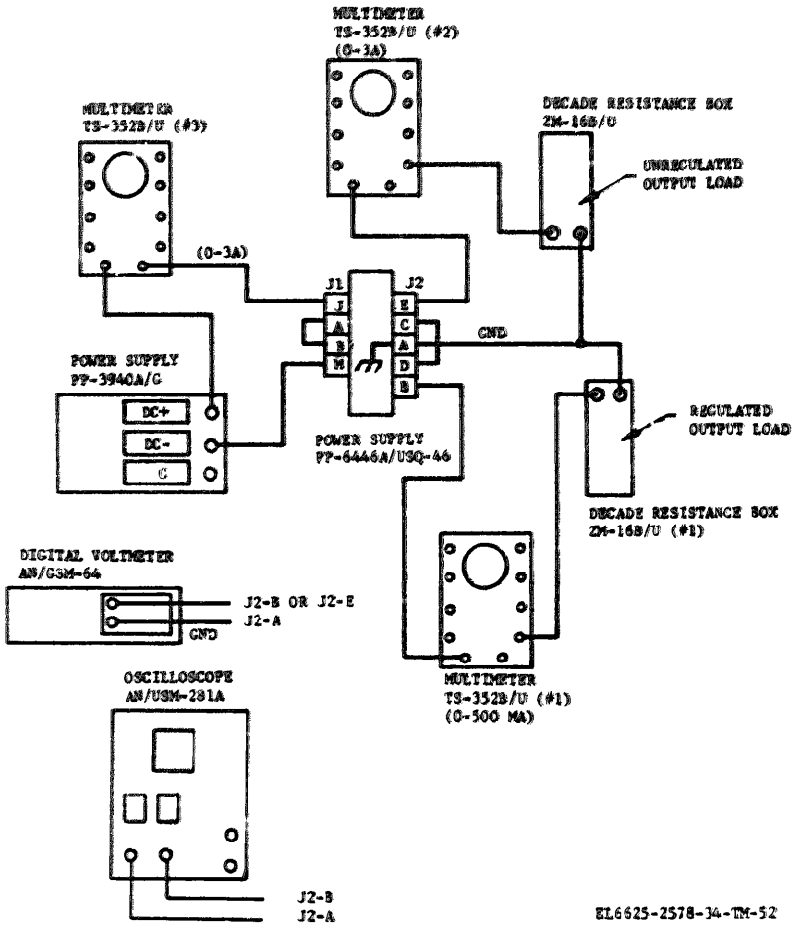



Figure 4-10. Dc mode voltage regulation test setup.

Chart 4-9. Dc Mode Voltage Regulation Test Procedure

| Step No. | Test equipment control settings | Power supply control settings | Procedure | Performance standard |
|---|---|---|---|---|
| 1 | *AN/USM-281A*<br>TRIGGER LEVEL:<br>AUTO<br>TRIGGER SOURCE:<br>INT<br>SWEEP: 10 ms/cm<br>VERT: 0.2 V/cm<br>(X10 probe)<br>*AN/GSM-64*<br>RANGE: 100 vdc<br>*PP-3940A/G*<br>PWR: ON at 22 +0.1, −0 vdc<br>*TS-352B/U No. 1*<br>RANGE: 0–500 ma<br>*TS-352B/U No. 2*<br>RANGE: 0–3 A<br>*ZM-16B/U*<br>As required in procedure. | None | *a.* Adjust ZM–16B/U No. 1 load for regulated output voltage.<br>*b.* Adjust ZM–16B/U No. 2 load for unregulated output voltage.<br>*c.* Connect AN/GSM–64 positive lead to J2–B and negative lead to J2A.<br>*d.* Connect AN/GSM–64 positive lead to J2–E, negative lead to J2–A.<br>*e.* Set input voltage to +25.2 +0.2 −0 vdc and measure voltage J2–E.<br>*f.* Set input voltage to +33.0, +0 −0.2 vdc and measure voltage at J2–B.<br>*g.* Measure voltage at J2–E .....<br>*h.* Connect AN/USM–281A, "A" channel to J2–B and observe any instability. | *a.* Adjust for 400 ±10 ma on TS–352B/U No. 1.<br>*b.* Adjust for 1.0 ±0.05 A on TS–352B/U No. 2.<br>*c.* Voltage shall be + 11.5 to + 16.0 vdc.<br>*d.* Voltage must not be less than +19 vdc.<br>*e.* Voltage must be +22 to +33 vdc.<br>*f.* Voltage must be +11.5 to +16.0 vdc.<br>*g.* Voltage must be +22 to +33 vdc.<br>*h.* Instability is any condition of oscillation including 60-Hz input line or pickup from external sources. |

4-19. Dc Mode Current Drain Test Procedure

*a. Test Equipment and Material.*

(1) Digital Voltmeter AN/GSM-64.

(2) Dc Ammeter TS-352B/U (3 required).

(3) Decade Resistance Box ZM-16B/U (2 required.

(4) Power Supply PP-3940A/G.

*b. Test Connections and Conditions.* Connect the equipment as shown in figure 4-10. The AN/USM-281A is not used in this test.

*c. Procedure.* Perform steps of chart 4-10.

Chart 4-10. DeMode Current Drain Test Procedure

| Step No. | Test equipment control settings | Power supply control settings | Procedure | Performance standard |
|---|---|---|---|---|
| 1 | *AN/GSM-64*<br>RANGE: 100 vdc<br>*PP-3940A/G*<br>PWR: ON at +28.0 +0, −0.3 vdc.<br>*TS-352B/U No. 1*<br>RANGE: 0–500 ma<br>*TS-352B/U No. 2*<br>RANGE: 0–3 A<br>*TS-352B/U No. 3*<br>RANGE: 0–3 A<br>*ZM-16B/U No. 1 & No. 2*<br>As required in procedure. | None | a. Adjust ZM-16B/U No. 1 load for regulated output voltage.<br>b. Adjust ZM-16B/U No. load for unregulated output voltage.<br>c. Connect AN/GSM-64 positive lead to J2-B, negative lead to J2-A.<br>d. Observe reading on TS-352B/U No. 3. | a. Adjust for 400 ±10 ma on TS-352B/U No. 1.<br>b. Adjust for 1.0 ±0.05 A on TS-352B/U No. 2.<br>c. Voltage shall be +11.5 to +16.0 vdc.<br>d. Current reading shall not exceed 1.75 A. |

4-20. Ac Mode Voltage Regulation Test Procedure

***a. Test Equipment and Material.***

**(1) Oscilloscope AN/USM-281A.**

**(2) Digital Voltmeter AN/GSM-64.**

**(3) Dc Ammeter TS-352B/U (2 required).**

**(4) Decade Resistance ZM-16M/U (2 required).**

**(5) Ac Ammeter, ME-65A/U.**

**(6) Variac Autotransformer CN-16/U.**

***b. Test Connections and Conditions.*** **Connect equipment as shown in figure 4-11.**

***c. Procedure.*** **Perform steps of chart 4-11.**

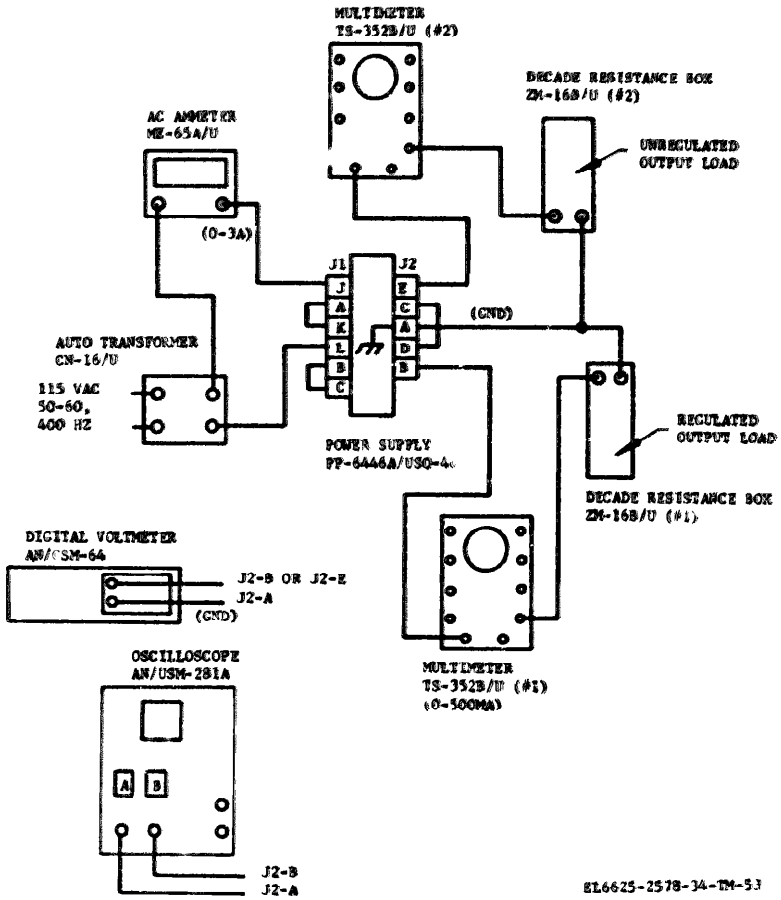



Figure 4-11. Ac mode voltage regulation test setup.

Chart 4-11. Ac Mode Voltage Regulation Test Procedure

| Step No. | Test equipment control settings | Power supply control settings | Procedure | Performance standard |
|---|---|---|---|---|
| 1 | *AN/USM-281A*<br>TRIGGER LEVEL: AUTO<br>TRIGGER SOURCE: INT<br>SWEEP: 10 ms/cm<br>VERT: 50 ma/cm<br>*AN/GMS-64*<br>RANGE: 100<br>*TS-352B/U No. 1*<br>RANGE: 0-500 ma<br>*TS-352B/U No. 2*<br>RANGE: 0-3 A<br>*ZM-16B/U No. 1 & No. 2*<br>As required in procedure.<br>*CN-16/U*<br>RANGE: 100 + 1.0, −0 vac. | None | *a.* Adjust ZM-16B/U No. 1 load for regulated output voltage.<br>*b.* Adjust ZM-16B/U No. 2 load for unregulated output voltage.<br>*c.* Connect AN/GSM-64 positive lead to J2-B and negative lead to J2-A.<br>*d.* Connect AN/GSM-64 positive lead to J2-E, negative lead to J2-A.<br>*e.* Set input voltage to 105 +1.0 −0 vdc and measure voltage at J2-E.<br>*f.* Set input voltage to 132 +0 −1.3 vac and measure voltage at J2-B.<br>*g.* Measure voltage at J2-E<br>*h.* Connect AN/USM-281A, "A" channel to J2-B and observe any instability. | *a.* Adjust for 400 ± 10 ma on TS-352B/U No. 1.<br>*b.* Adjust for 1.0 ± 0.05 A on TS-352B/U No. 2.<br>*c.* Voltage shall be +11.5 to +16.0 vdc.<br>*d.* Voltage shall not be less than +19 vdc.<br>*e.* Voltage shall be +22 to +33 vdc.<br>*f.* Voltage shall be +11.5 to +16.0 vdc.<br>*g.* Voltage shall be +22 to +33 vdc.<br>*h.* Instability is any condition of oscillation including 60-Hz input line or pickup from external sources. |

4-21. Ac Mode Current Drain Test Procedure

*a. Test Equipment and Material.*

**(1) Digital Voltmeter AN/GSM-64.**

**(2) Dc Ammeter TS-352B/U (2 required).**

**(3) Decade Resistance Box ZM-16B/U (2 required).**

**(4) Ac Ammeter ME-65A/U.**

**(5) Variac Autotransformer CN-16/U.**

*b. Test Connections and Conditions.* **Connect equipment as shown in figure 4-11. The AN/USM-281A is not used in this test.**

*c. Procedure.* **Perform steps of chart 4-12.**

## Section VIII. GENERAL SUPPORT REMOVAL OR REPLACEMENT OF POWER SUPPLY COMPONENTS

### 4-22. General

Power supply components not covered in chapter 3 may be repaired or replaced at this maintenance level except for feedthrough terminals on connector J2. These terminals are sweated in place, thereby requiring tools found only at the depot maintenance level. The following paragraphs describe removal or replacement procedures for general support components.

### 4-23. Removal or Replacement of Transformer 2T1

(fig. 3-15(1)).

*a. Disassembly.*

(1) Remove the 22 panhead screws (4) and 22 flat washers (5) securing the cover plate (6) and remove cover plate to extent allowed by wires connected to 2J2 feedthrough terminals.

(2) Unsolder wires to 2T1 (8) noting their terminal connection, and mark wires as required.

(3) Remove four panhead screws (9) and four flat washers (10) to remove 2T1 (8).

*b. Reassembly.*

(1) Position 2T1 (8) in place and secure with four flat washers (10) and four panhead screws (9).

(2) Connect wires to terminals of 2T1 (8) as marked during disassembly.

(3) Position cover plate (6) and secure with 22 flat washers (5) and 22 panhead screws (4).

### 4-24. Removal or Replacement of Choke 2L1

(fig. 3-15(1)).

*a. Disassembly.*

(1) Perform step (1) of paragraph 4–23*a*.

(2) Unsolder wires to 2L1 (11) noting their terminal connection, and mark wires as required.

(3) Remove three panhead screws (12) and three flat washers (13); then remove 2L1 (11).

*b. Reassembly.*

(1) Position 2L1 (11) in place and secure with three flat washers (13) and three panhead screws (12).

(2) Connect wires to terminals of 2L1 (11) as marked during disassembly.

(3) Perform step (3) of paragraph 4–23*b*.

### 4-25. Removal or Replacement of Capacitors 2C1 and 2C2

(fig. 3-15(1)).

*a. Disassembly.*

(1) Perform step (1) of paragraph 4–23*a*.

(2) Unsolder wires to 2C1 (14) and 2C2 (15), noting their terminal connection, and mark wires as required.

(3) Remove two panhead screws (16) and two lockwashers (17) to remove capacitor mounting brackets (18) with capacitor 2C1 (14) and 2C2 (15).

*b. Reassembly.*

(1) Place capacitors 2C1 (14) and 2C2 (15) in the mounting brackets (18).

(2) Position mounting brackets (18) in place and secure with two flat washers (17) and two panhead screws (16).

(3) Connect wires to 2C1 (14) and 2C2 (15) as marked during disassembly.

(4) Perform step (3) of paragraph 4–23*b*.

### 4-26. Removal or Replacement of Connector Assembly J1

(fig. 3-15(1) and (2)).

*a. Disassembly.*

(1) Perform step (1) of paragraph 4–23*a*.

(2) Unsolder wires to connector assembly J1 (19) noting their terminal connections, and mark wires as required.

(3) Loosen and remove locking nut (20) (sheet ② of 2) and remove J1 (19). The locking nut is supplied as part of assembly J1, therefore does not need to be saved when replacing J1.

*b. Reassembly.*

(1) Position connector assembly J1 (19) in place and secure with locking nut (20).

(2) Connect wires to assembly J1 (19) as marked during disassembly.

(3) Perform step (3) of paragraph 4–23*b*.

4-27. Removal or Replacement of Fuseholders for F1, F2, and F3 (fig. 3-15(2)).

*a. Disassembly.*

**(1) Perform step (1) of paragraph 4–23a.**

**(2) Unsolder wires to applicable fuse holder (21) noting terminal connections and mark wires as required.**

**(3) Remove retaining nut (22) (sheet 1 of 2) of applicable fuse holder (21) and remove fuseholder (21).**

*b. Reassembly.*

**(1) Position applicable fuse holder (21) in place and secure with retaining nut (22).**

**(2) Connect wires to applicable fuse holder (21) terminals as marked during disassembly.**

**(3) Perform step (3) of paragraph 4–23b.**

4-28. Removal or Replacement of Component Plate Assembly 2A5 (fig. 3-15(1)).

*a. Disassembly.*

**(1) Perform step (1) of paragraph 4–23a.**

**(2) Unsolder wires to terminals 2A5E12, 14, 18, 21, 24, 25 and 26 of the component plate assembly (23) and mark the wires as required.**

**(3) Remove four panhead screws (24), four lockwashers (25) and four flat washers (26) to remove component plate assembly (23).**

*b. Reassembly.*

**(1) Position component plate assembly (23) in place and secure with four flat washers (26), four lockwashers (25) and four panhead screws (24).**

**(2) Connect wires to terminals 2A5E12, 14, 18, 21, 24 and 25 as marked during disassembly.**

**(3) Perform step (3) of paragraph 4–23b.**

4-29. Removal or Replacement of Component Board 2A5A2 (fig. 3-15(1)).

*a. Disassembly.*

**(1) Perform step (1) of paragraph 4–23a and all steps of paragraph 4–28a.**

**(2) Unsolder interconnecting leads of components between component plate assembly (23) and component board (27) and mark leads as required.**

**(3) Remove screw terminal (28), panhead screw (29), lockwasher (30) and flat washer (31) to remove component board (27).**

*b. Reassembly.*

**(1) Position component board (27) in place on standoffs (32) and secure with screw terminal (28), flat washer (31), lockwasher (30), and panhead screw (29).**

**(2) Connect component leads between component plate assembly (23) and component board (27) as marked during disassembly.**

**(3) Perform all steps of paragraph 4–28b and step (3) of paragraph 4–23b.**

# CHAPTER 5

# DEPOT REPAIR AND OVERHAUL

## 5-1. General

**Module testing, troubleshooting and repair, and system overhaul is accomplished by depot level maintenance personal. Depot repair and overhaul is described in DMWR 11-6625-2578 manual and is available only at depot level.**

# CHAPTER 6

# FINAL ILLUSTRATIONS

## 6-1. General

This chapter contains all fold-out illustrations, which include wiring, block, and schematic diagrams.

## 6-2. Wiring Diagram Color Codes

All module connector plugs (1A1 chassis mounted) have their wires molded to the connector and the wires are all color coded in accordance with MIL–STD–681, system 1. All module connector wires are No. 26 AWG stranded. Table 6–1 lists the module connector color code sequence for connectors with up to 37 pins, which is the largest connector used for the radio test set modules. Connector pins not noted on the wiring diagram are spares. Color code and size of remaining chassis wiring is listed in table 6–2.

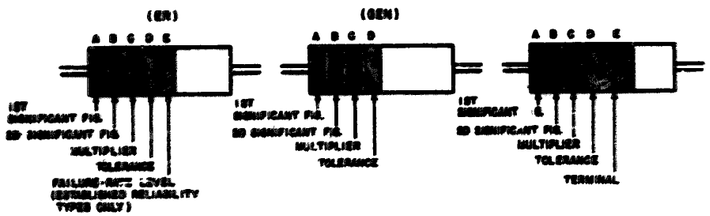
Table 6-1. Module Connector Wiring Color Code Sequence.

| *Pin* | *Base color* | *First stripe or bank* | *Second stripe or bank* |
|---|---|---|---|
| 1 | Black | | |
| 2 | Brown | | |
| 3 | Red | | |
| 4 | Orange | | |
| 5 | Yellow | | |
| 6 | Green | | |
| 7 | Blue | | |
| 8 | Violet | | |
| 9 | Gray | | |
| 10 | White | | |
| 11 | White | Black | |
| 12 | White | Brown | |
| 13 | White | Red | |
| 14 | White | Orange | |
| 15 | White | Yellow | |
| 16 | White | Green | |
| 17 | White | Blue | |
| 18 | White | Violet | |
| 19 | White | Gray | |
| 20 | White | Black | Brown |
| 21 | White | Black | Red |
| 22 | White | Black | Orange |
| 23 | White | Black | Yellow |
| 24 | White | Black | Green |
| 25 | White | Black | Blue |
| 26 | White | Black | Violet |
| 27 | White | Black | Gray |
| 28 | White | Brown | Red |
| 29 | White | Brown | Orange |
| 30 | White | Brown | Yellow |
| 31 | White | Brown | Green |
| 32 | White | Brown | Blue |
| 33 | White | Brown | Violet |
| 34 | White | Brown | Gray |
| 35 | White | Red | Orange |
| 36 | White | Red | Yellow |
| 37 | White | Red | Green |

Table 6-2. Chassis Wiring Color Code and Size.

| Color code | Wire type and size | From— | To— |
|---|---|---|---|
| Yellow | #26 AWG Strd. | 1A1A16-E2 | 1A1A18E1-Gnd |
| White | RG188 Coax | 1A1A16-E3 | 1A1A10J2 |
| | Resistor | 1A1A16-E1 | 1A1-E7 |
| Yellow | #26 AWG Strd. | 1A1A17-E1 | 1A1A18F1-2 (Sleeve) |
| Yellow | #26 AWG Strd. | 1A1A17-E7 | 1A1A18TB1-1 |
| Yellow | #26 AWG Strd. | 1A1A17-E5 | 1A1A18TB1-2 |
| Yellow | #26 AWG Strd. | 1A1A17-E2 | 1A1A18TB1-5 |
| Yellow | #26 AWG Strd. | 1A1A17-E2 | 1A1-E7 |
| Yellow | #26 AWG Strd. | 1A1A17-E1 | 1A5-E5 |
| Red | #26 AWG Strd. | 1A1A18S7B(R)-10 | 1A1A18F1-2 (Tip) |
| Yellow | #26 AWG Strd. | 1A1-E3 | 1A1A18TB2-1 |
| Black | #20 AWG Strd. | 1A1P1-3 | 1A1A18S7A(F)-8 |
| White | #20 AWG Strd. | 1A1P1-4 | 1A1A18S7A(F)-10 |
| Black | #20 AWG Strd. | 1A1P1-1 | 1A1A18E1 (Gnd) |
| Red | #20 AWG Strd. | 1A1P1-2 | 1A1A18S7B(R)-8 |
| Yellow | #26 AWG Strd. | 1A1-E6 | 1A1A17-E7 |
| | #26 AWG Buss | 1A1-E4 | 1A1-E5 |
| | #26 AWG Buss | 1A1-E1 | 1A1-E2 |
| | #26 AWG Buss | 1A1-E2 | 1A1-E3 |
| Black | #16 AWG Strd. | 1A1-E6 | 1A1A18E1 (Gnd) |
| Green | #16 AWG Strd. | 1A1-E2 | 1A1A3J1-6 |
| Yellow | #26 AWG Strd. | 1A1A18R1-2 | 1A1A18E1-(Gnd) |
| Yellow | #26 AWG Strd. | 1A1A18S1(R)-1 | 1A1A18S2A(R)-4 |
| Yellow | #26 AWG Strd. | 1A1A18S1(R)-2 | 1A1A 8S2B(R)-4 |
| Yellow | #26 AWG Strd. | 1A1A18S1(R)-3 | 1A1A18S2C(R)-4 |
| Yellow | #26 AWG Strd. | 1A1A18S1(R)-4 | 1A1A18TB3-25 |
| Yellow | #26 AWG Strd. | 1A1A18S2A(R)-2 | 1A1A18TB2-16 |
| Yellow | #26 AWG Strd. | 1A1A18S2A(R)-5 | 1A1A18TB2-6 |
| Yellow | #26 AWG Strd. | 1A1A18S2A(R)-8 | 1A1A18TB2-14 |
| Yellow | #26 AWG Strd. | 1A1A18S2A(R)-11 | 1A1A18TB2-4 |
| | #26 AWG Buss | 1A1A18S2A(R)-11 | 1A1A18S2B(R)-11 |
| Yellow | #26 AWG Strd. | 1A1A18S2B(R)-2 | 1A1A18TB2-12 |
| Yellow | #26 AWG Strd. | 1A1A18S2B(R)-5 | 1A1A18TB2-2 |
| Yellow | #26 AWG Strd. | 1A1A18S2B(R)-8 | 1A1A18TB2-10 |
| | #26 AWG Buss | 1A1A18S2B(R)-8 | 1A1A18S2C(R)-8 |
| Yellow | #26 AWG Strd. | 1A1A18S2C(R)-11 | 1A1A18TB2-1 |
| Yellow | #26 AWG Strd. | 1A1A18S2C(R)-2 | 1A1A18TB2-8 |
| | #26 AWG Buss | 1A1A18S2C(F)-11 | 1A1A18S2B(F)-2 |
| | #26 AWG Buss | 1A1A18S2B(F)-11 | 1A1A18S2A(F)-11 |
| Yellow | #26 AWG Strd. | 1A1A18S2A(F)-11 | 1A1A18S3B(R)-2 |
| | #26 AWG Buss | 1A1A18S3B(R)-2 | 1A1A18S3B(F)-2 |
| | #26 AWG Buss | 1A1A18S3B(F)-2 | 1A1A18S3A(R)-2 |
| | #26 AWG Buss | 1A1A18S3A(R)-2 | 1A1A18S3A(F)-2 |
| Yellow | #26 AWG Strd. | 1A1A18S3A(F)-2 | 1A1A18S4B(R)-2 |
| | #26 AWG Buss | 1A1A18S4B(R)-2 | 1A1A18S4B(F)-2 |
| | #26 AWG Buss | 1A1A18S4B(F)-2 | 1A1A18S4A(R)-2 |
| | #26 AWG Buss | 1A1A18S4A(R)-2 | 1A1A18S4A(F)-2 |
| Yellow | #26 AWG Strd. | 1A1A18S4A(F)-2 | 1A1A18E1-(Gnd) |
| Yellow | #26 AWG Strd. | 1A1A18S7A(R)-2 | 1A1A18TB3-6 |
| Yellow | #26 AWG Strd. | 1A1A18S7A(R)-3 | 1A1A18TB3-8 |
| Yellow | #26 AWG Strd. | 1A1A18S7A(R)-12 | 1A1A18S9(R)-5 |
| Yellow | #26 AWG Strd. | 1A1A18S9(R)-5 | 1A1A18S8(R)-6 |
| | #26 AWG Buss (Sleeved) | 1A1A18S8(R)-6 | 1A1A18S8(R)-8 |
| Yellow | #26 AWG Strd. | 1A1A18S8(R)-8 | 1A1A18TB3-30 |
| | #26 AWG Buss (Sleeved) | 1A1A18S8(R)-5 | 1A1A18S8(R)-7 |
| | #26 AWG Buss (Sleeved) | 1A1A18S8(R)-7 | 1A1A18S8(R)-9 |
| Yellow | #26 AWG Strd. | 1A1A18S8(R)-9 | 1A1A18E1-(Gnd) |
| Yellow | #26 AWG Strd. | 1A1A18S11-1 | 1A1A18TB3-30 |
| Yellow | #26 AWG Strd. | 1A1A18S10(R)-5 | 1A1A18M1-1(-) |

| Color code | Wire type and size | From— | To— |
|---|---|---|---|
| Yellow | #26 AWG Strd. | 1A1A18S10(R)-11 | 1A1A18M1-2(+) |
| | Sleeved braid | 1A1A18M1-G | 1A1A18E2-(Gnd) |
| Yellow | #26 AWG Strd. | 1A1A18S5(F)-10 | 1A1A18S6(F)-9 |
| | #26 AWG Buss | 1A1A18S8(R)-2 | 1A1A18S8(R)-3 |
| | #26 AWG Buss (Sleeved) | 1A1A18S8(R)-4 | 1A1A18S8(R)-1 |
| White | #26 AWG Strd. | 1A1A18S72(R)-4 | 1A1A18TB3-1 |
| Yellow | #26 AWG Strd. | 1A1A18TB1-1 | 1A1A18TB3-27 |
| | #26 AWG Buss | 1A1A18TB1-2 | 1A1A18TB1-3 |
| | #26 AWG Buss | 1A1A18TB1-3 | 1A1A18TB1-4 |
| Yellow | #26 AWG Strd. | 1A1A18TB1-4 | 1A1A18TB3-30 |
| Yellow | #26 AWG Strd. | 1A1A18TB1-5 | 1A1A18TB3-28 |
| | #26 AWG Buss | 1A1A18TB2-2 | 1A1A18TB2-3 |
| | #26 AWG Buss | 1A1A18TB2-4 | 1A1A18TB2-5 |
| | #26 AWG Buss | 1A1A18TB2-6 | 1A1A18TB2-7 |
| | #26 AWG Buss | 1A1A18TB2-8 | 1A1A18TB2-9 |
| | #26 AWG Buss | 1A1A18TB2-10 | 1A1A18TB2-11 |
| | #26 AWG Buss | 1A1A18TB2-12 | 1A1A18TB2-13 |
| | #26 AWG Buss | 1A1A18TB2-14 | 1A1A18TB2-15 |
| | #26 AWG Buss | 1A1A18TB2-16 | 1A1A18TB2-17 |
| Black | #16 AWG Buss | 1A1A18TB2-18 | 1A1A18E1-Gnd |
| | #26 AWG Buss | 1A1A18TB3-3 | 1A1A18TB3-4 |
| | #26 AWG Buss | 1A1A18TB3-5 | 1A1A18TB3-6 |
| | #26 AWG Buss | 1A1A18TB3-7 | 1A1A18TB3-8 |
| | #26 AWG Buss | 1A1A18TB3-9 | 1A1A18TB3-10 |
| | #26 AWG Buss | 1A1A18TB3-10 | 1A1A18TB3-11 |
| | #26 AWG Buss | 1A1A18TB3-12 | 1A1A18TB3-13 |
| | #26 AWG Buss | 1A1A18TB3-14 | 1A1A18TB3-15 |
| | #26 AWG Buss | 1A1A18TB3-15 | 1A1A18TB3-16 |
| | #26 AWG Buss | 1A1A18TB3-17 | 1A1A18TB3-18 |
| | #26 AWG Buss | 1A1A18TB3-19 | 1A1A18TB3-20 |
| | #26 AWG Buss | 1A1A18TB3-21 | 1A1A18TB3-22 |
| | #26 AWG Buss | 1A1A18TB3-23 | 1A1A18TB3-24 |
| Yellow | #26 AWG Strd. | 1A1A18TB3-31 | 1A1A9J1-27 |
| Yellow | #26 AWG Strd. | 1A1A18TB3-32 | 1A1A18J1 |
| Yellow | #26 AWG Strd. | 1A1A18TB3-33 | 1A1A14J1-23 |
| Yellow | #26 AWG Strd. | 1A1A18TB3-29 | 1A1A18E1-Gnd |
| Yellow | #26 AWG Strd. | 1A1A18TB3-28 | 1A1A18TB1-5 |
| Yellow | #26 AWG Strd. | 1A1A18T1-J1 | 1A1A18J3 |




COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS.

COLOR-CODE MARKING FOR FILM-TYPE RESISTORS.

TABLE I

COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS.

| BAND A | | BAND B | | BAND C | | BAND D | | BAND E | | |
|---|---|---|---|---|---|---|---|---|---|---|
| COLOR | FIRST SIGNIFICANT FIGURE | COLOR | SECOND SIGNIFICANT FIGURE | COLOR | MULTIPLIER | COLOR | RESISTANCE TOLERANCE (PERCENT) | COLOR | FAILURE RATE LEVEL | TERM. |
| BLACK | 0 | BLACK | 0 | BLACK | 1 | | | BROWN | M=1.0 | |
| BROWN | 1 | BROWN | 1 | BROWN | 10 | | | RED | P=0.1 | |
| RED | 2 | RED | 2 | RED | 100 | | | ORANGE | R=0.01 | |
| ORANGE | 3 | ORANGE | 3 | ORANGE | 1,000 | | | YELLOW | S=0.001 | |
| YELLOW | 4 | YELLOW | 4 | YELLOW | 10,000 | SILVER | ±10 (COMP TYPE ONLY) | WHITE | | SOLDERABLE |
| GREEN | 5 | GREEN | 5 | GREEN | 100,000 | GOLD | ±5 | | | |
| BLUE | 6 | BLUE | 6 | BLUE | 1,000,000 | RED | ±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY) | | | |
| PURPLE (VIOLET) | 7 | PURPLE (VIOLET) | 7 | | | | | | | |
| GRAY | 8 | GRAY | 8 | SILVER | 0.01 | | | | | |
| WHITE | 9 | WHITE | 9 | GOLD | 0.1 | | | | | |

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH.)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE.

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE.

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL (PERCENT FAILURE PER 1,000 HOURS). ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1-1/2 TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL.

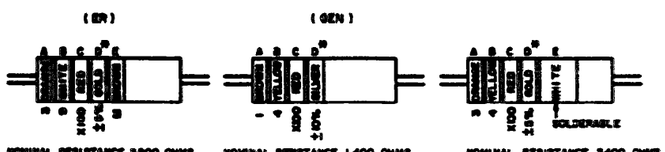
RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS (THESE ARE NOT COLOR CODES)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE:

2R7 = 2.7 OHMS  10R0 = 10.0 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED; IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS.

EXAMPLES OF COLOR CODING




NOMINAL RESISTANCE 3,900 OHMS
RESISTANCE TOLERANCE ±1%
FAILURE RATE LEVEL M

NOMINAL RESISTANCE 1,400 OHMS
RESISTANCE TOLERANCE ±10%

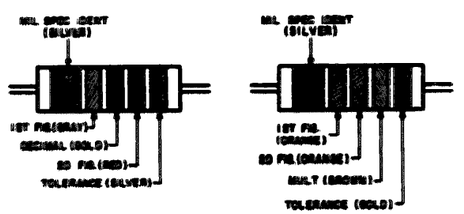
NOMINAL RESISTANCE 3,400 OHMS
RESISTANCE TOLERANCE ±1%
TERMINAL SOLDERABLE

COMPOSITION-TYPE RESISTORS.

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-STD.

A. COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS




(A) 8.2 UH ± 10%

(B) 330 UH ± 5%

COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES. AT A, AN EXAMPLE OF THE CODING FOR AN 8.2 UH CHOKE IS GIVEN. AT B, THE COLOR BANDS FOR A 330 UH INDUCTOR ARE ILLUSTRATED

TABLE II

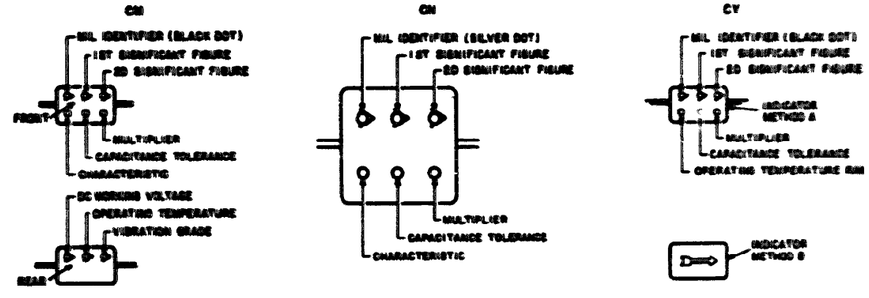
COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES.

| COLOR | SIGNIFICANT FIGURE | MULTIPLIER | INDUCTANCE TOLERANCE (PERCENT) |
|---|---|---|---|
| BLACK | 0 | 1 | |
| BROWN | 1 | 10 | 1 |
| RED | 2 | 100 | 2 |
| ORANGE | 3 | 1,000 | 3 |
| YELLOW | 4 | | |
| GREEN | 5 | | |
| BLUE | 6 | | |
| VIOLET | 7 | | |
| GRAY | 8 | | |
| WHITE | 9 | | |
| NONE | | | 20 |
| SILVER | | | 10 |
| GOLD | DECIMAL POINT | | 5 |

MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL

B. COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS.

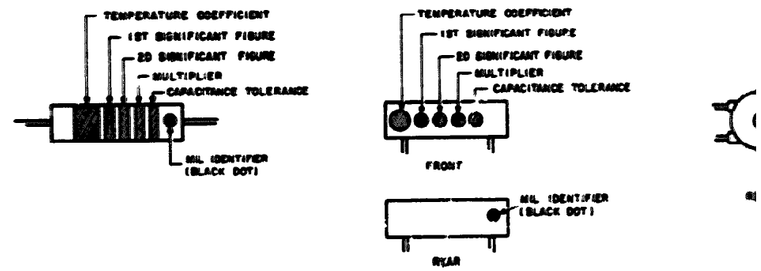
CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB.




MICA-DIELECTRIC

PAPER-DIELECTRIC

GLASS-DIELECTRIC, GLASS CASE

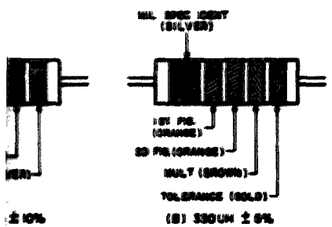



AXIAL LEAD

RADIAL LEAD

C COLOR CO

Figure 6-1. Color code marking for MIL-STD capacitors, inductors, and resistors.




TUBULAR ENCAPSULATED R.F. CHOKES. AT A, AN EXAMPLE OF B AN 0.33UH CHOKE IS GIVEN AT B, THE COLOR BANDS FOR B ARE ILLUSTRATED.

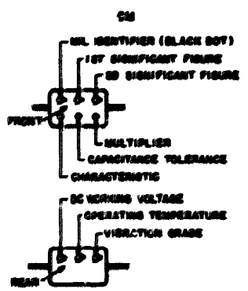
TABLE 2
CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES.

| BAR | SIGNIFICANT FIGURE | MULTIPLIER | INDUCTANCE TOLERANCE (PERCENT) |
|---|---|---|---|
| | 0 | 1 | |
| | 1 | 10 | 1 |
| | 2 | 100 | 2 |
| | 3 | 1,000 | 3 |
| | 4 | | |
| | 5 | | |
| | 6 | | |
| | 7 | | |
| | 8 | | |
| | 9 | | |
| | | | 20 |
| | | | 10 |
| | DECIMAL POINT | | 5 |

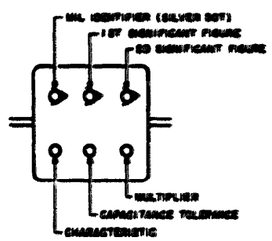
LISR IS THE FACTOR BY WHICH THE TWO COLOR FIGURES LTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE BAR.

CODE MARKING FOR MILITARY STANDARD INDUCTORS.

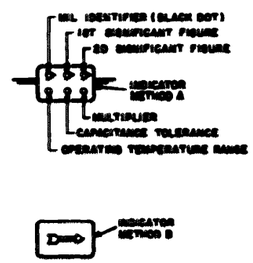
CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB.



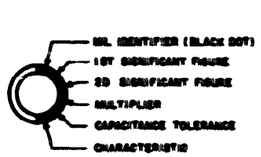

MICA-DIELECTRIC




PAPER-DIELECTRIC




GLASS-DIELECTRIC, GLASS CASE




MICA, BUTTON TYPE

TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB.

| COLOR | MIL ID | 1ST SIG FIG. | 2D SIG FIG. | MULTIPLIER | CAPACITANCE TOLERANCE CM | CN | CY | CB | CHARACTERISTIC CM | CN | CB | DC WORKING VOLTAGE CM | OPERATING TEMP RANGE CY, CB | VIBRATION GRADE CM |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BLACK | CM,CY CB | 0 | 0 | 1 | | | ±20% | ±20% | | A | | | $-55^{\circ}_{10}+70^{\circ}$C | 10-55 C |
| BROWN | | 1 | 1 | 10 | | | | | B | E | B | | | |
| RED | | 2 | 2 | 100 | ±2% | | ±1% | ±2% | C | | | | $-55^{\circ}_{10}+85^{\circ}$C | |
| ORANGE | | 3 | 3 | 1,000 | | ±30% | | | D | | D | 300 | | |
| YELLOW | | 4 | 4 | 10,000 | | | | | E | | | | $-55^{\circ}_{10}+125^{\circ}$C | 10-2,000 C |
| GREEN | | 5 | 5 | | ±5% | | | | F | | | 500 | | |
| BLUE | | 6 | 6 | | | | | | | | | | $-55^{\circ}_{10}+150^{\circ}$C | |
| PURPLE (VIOLET) | | 7 | 7 | | | | | | | | | | | |
| GREY | | 8 | 8 | | | | | | | | | | | |
| WHITE | | 9 | 9 | | | | | | | | | | | |
| GOLD | | | | 0.1 | | | ±5% | ±5% | | | | | | |
| SILVER | CN | | | | ±10% | ±20% | ±10% | ±10% | | | | | | |

C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS

TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC.

| COLOR | TEMPERATURE COEFFICIENT[4] | 1ST SIG FIG. | 2D SIG FIG. | MULTIPLIER[1] | CAPACITANCE TOLERANCE: CAPACITANCES OVER 10 UUF | CAPACITANCES 10 UUF OR LESS | MIL ID |
|---|---|---|---|---|---|---|---|
| BLACK | 0 | 0 | 0 | 1 | | ±2.0 UUF | CC |
| BROWN | −30 | 1 | 1 | 10 | ±1% | | |
| RED | −80 | 2 | 2 | 100 | ±2% | ±0.25 UUF | |
| ORANGE | −150 | 3 | 3 | 1,000 | | | |
| YELLOW | −220 | 4 | 4 | | | | |
| GREEN | −330 | 5 | 5 | | ±5% | ±0.5 UUF | |
| BLUE | −470 | 6 | 6 | | | | |
| PURPLE (VIOLET) | −750 | 7 | 7 | | | | |
| GREY | | 8 | 8 | 0.01 | | | |
| WHITE | | 9 | 9 | 0.1 | ±10% | | |
| GOLD | +100 | | | | | ±1.0 UUF | |
| SILVER | | | | | | | |

1 THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF

2 LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS: MIL-C-5, MIL-C-250, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY

3 LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D

4 TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE



Figure 6-1. Color code marking for MIL-STD capacitors, inductors, and resistors.

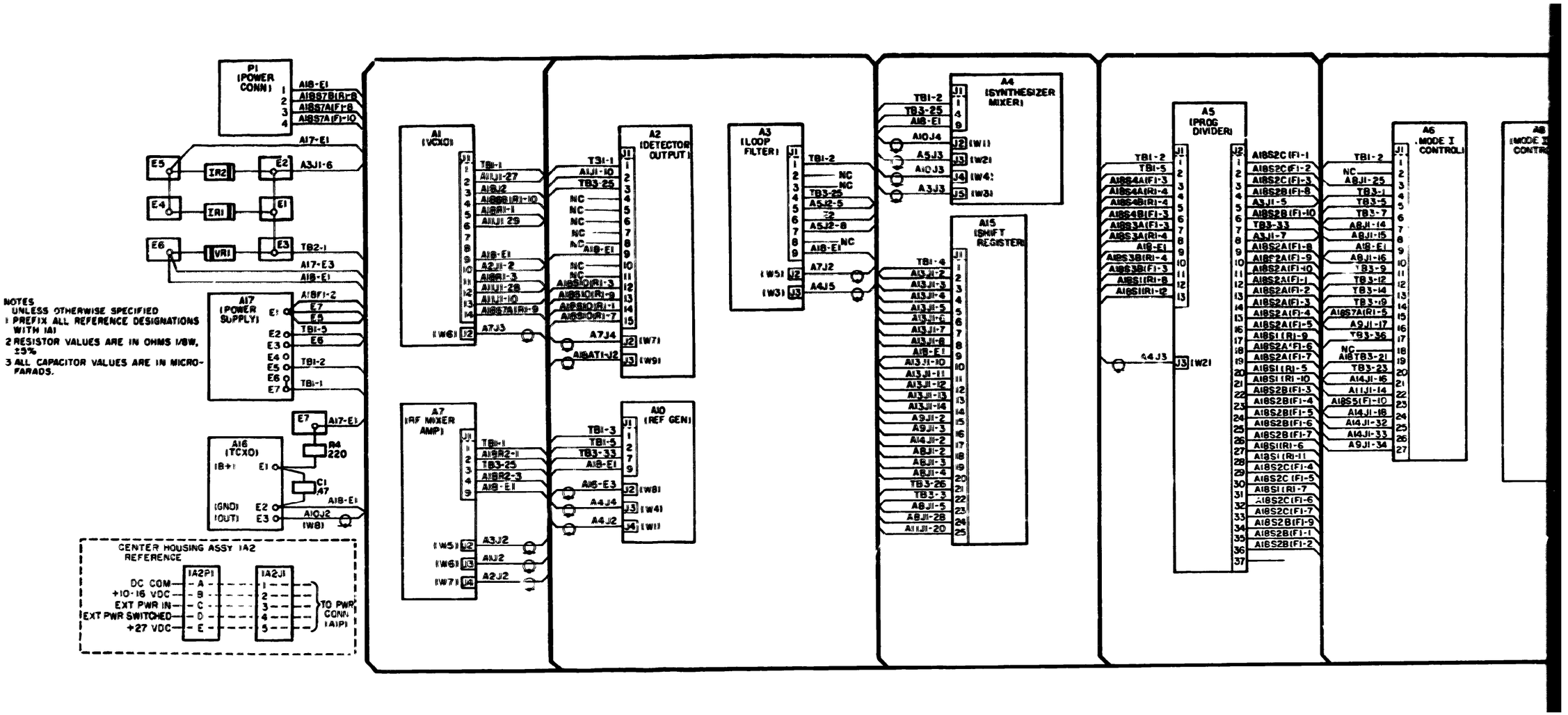



Figure 6-2(1). Test set power and control circuit, interconnection, wiring diagram (sheet 1 of 2).

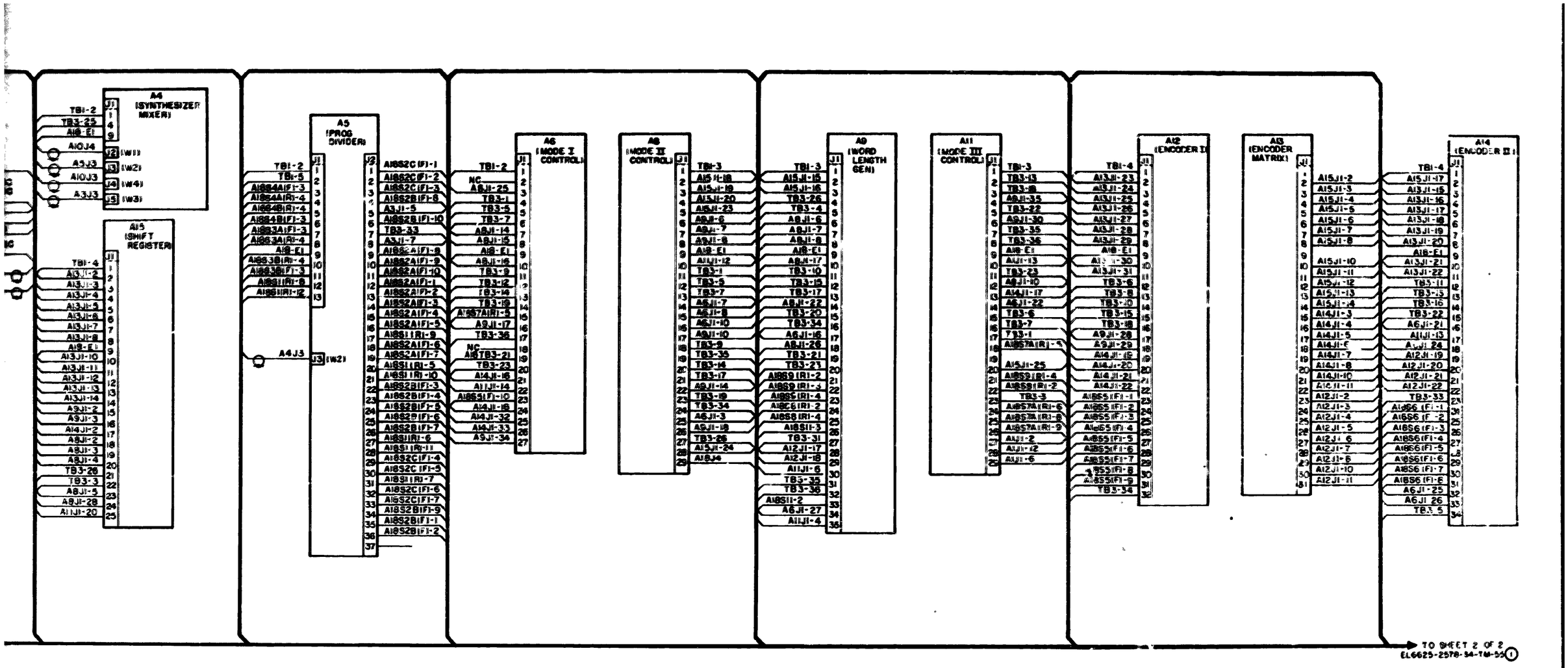



Figure 6-2(1). Test set power and control circuit, interconnection, wiring diagram (sheet 1 of 2).

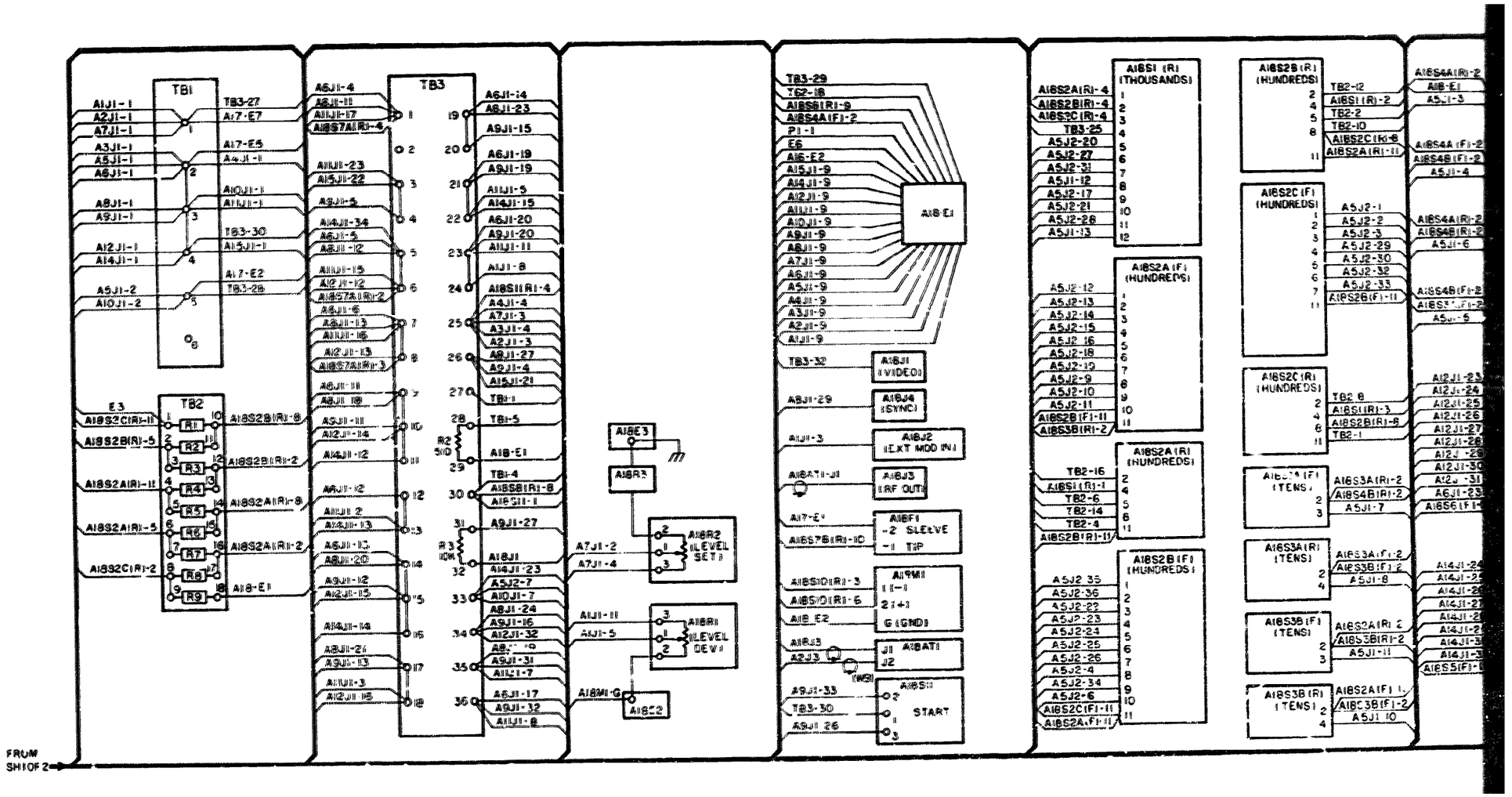



Figure 6-2(2). Test set power and control circuit, interconnection, wiring diagram (sheet 2 of 2).

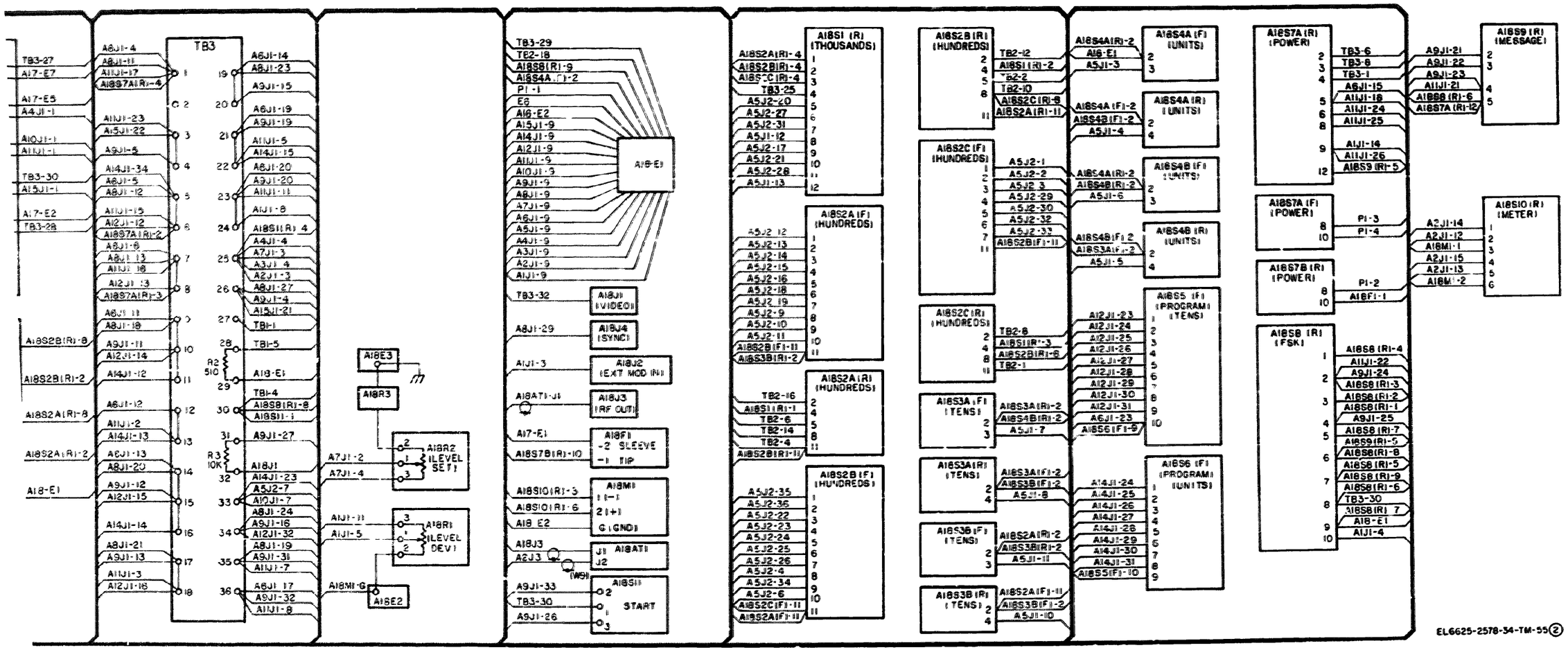



Figure 6-2(2). Test set power and control circuit, interconnection, wiring diagram (sheet 2 of 2).

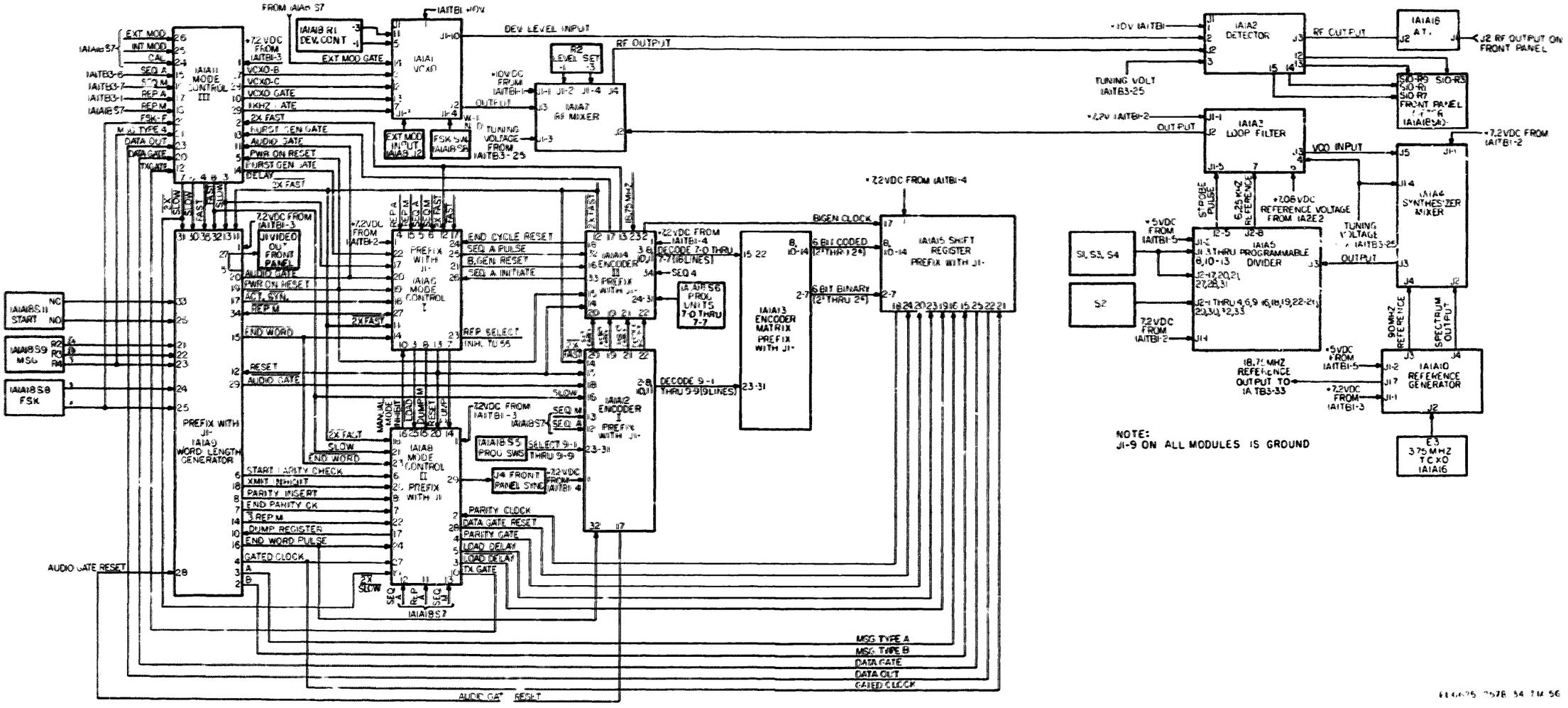



Figure 6-3. Test set, block diagram.

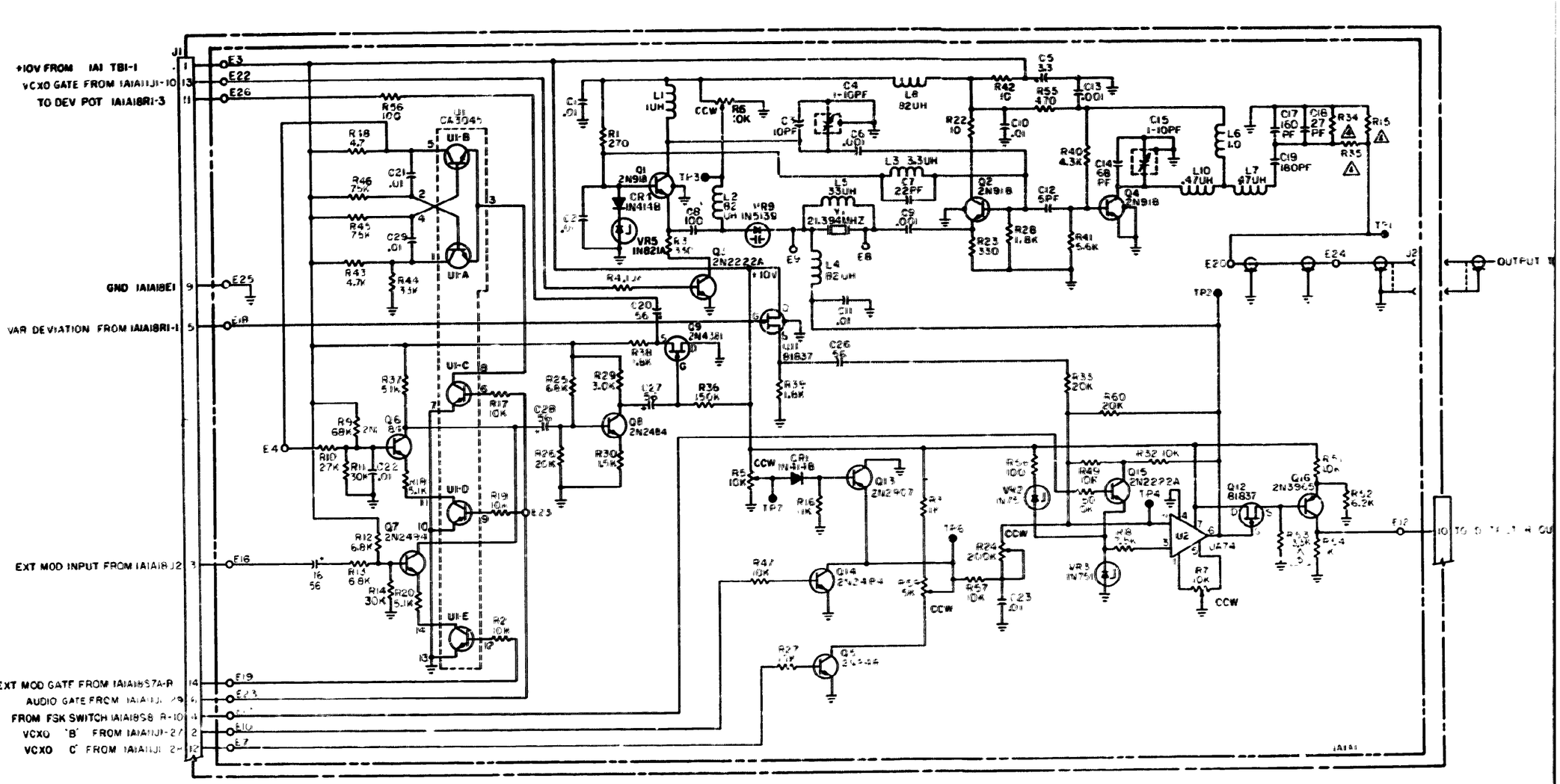



Figure 6-4. VCXO (1A1A1), schematic diagram.

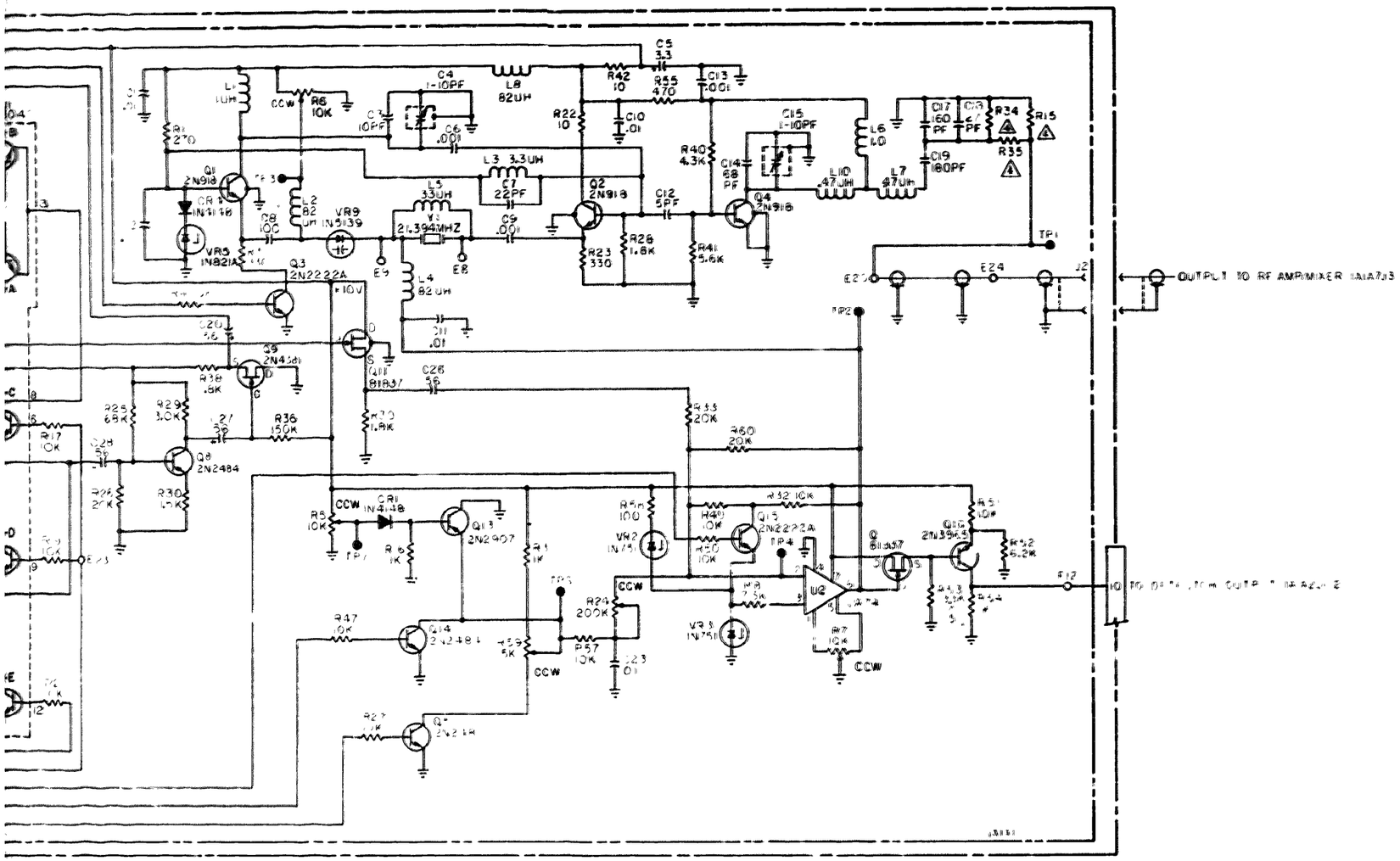



Figure 6-4. VCXO (1A1A1), schematic diagram.

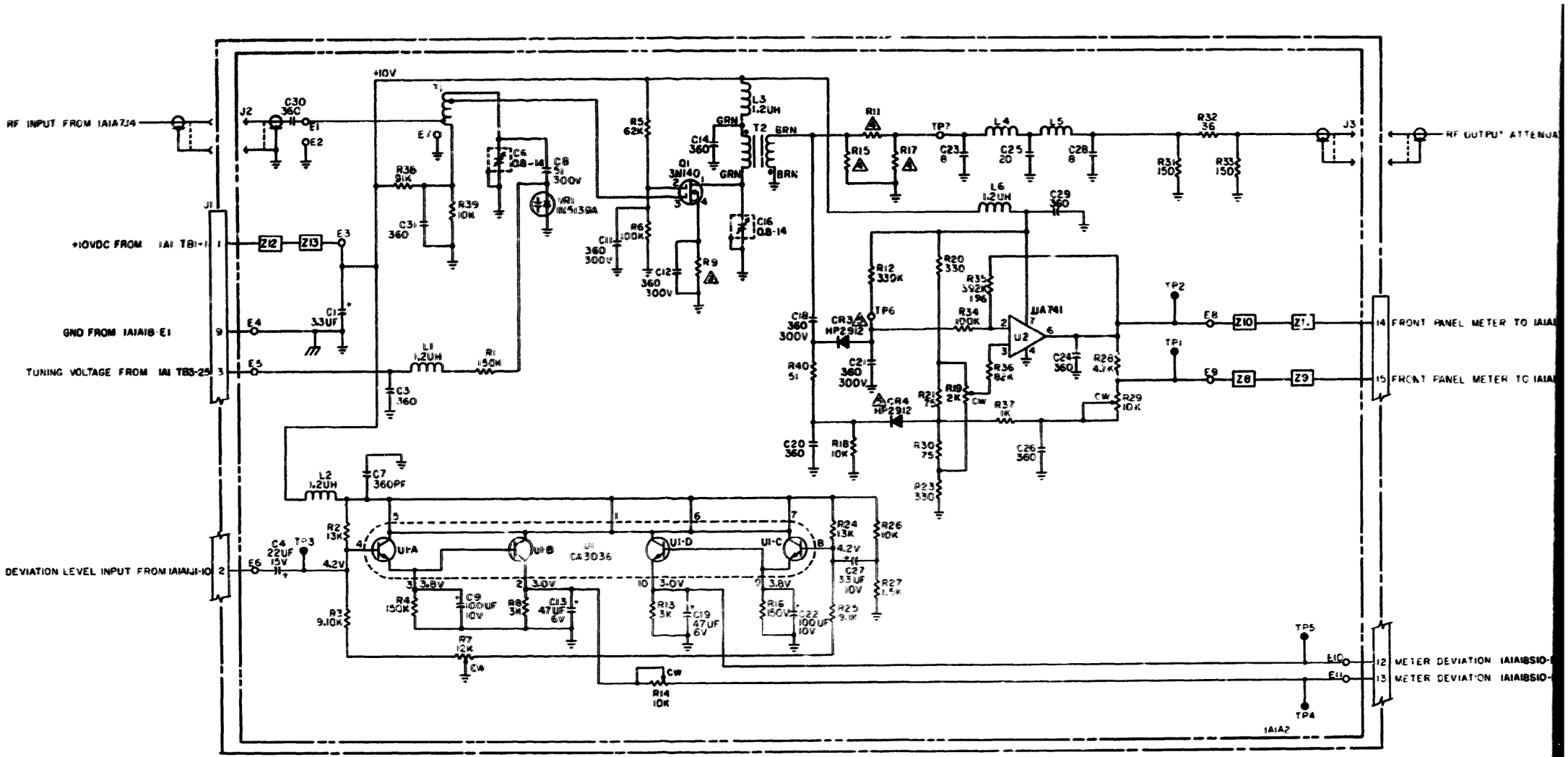



Figure 6-5. Detector output (1A1A2), schematic diagram.

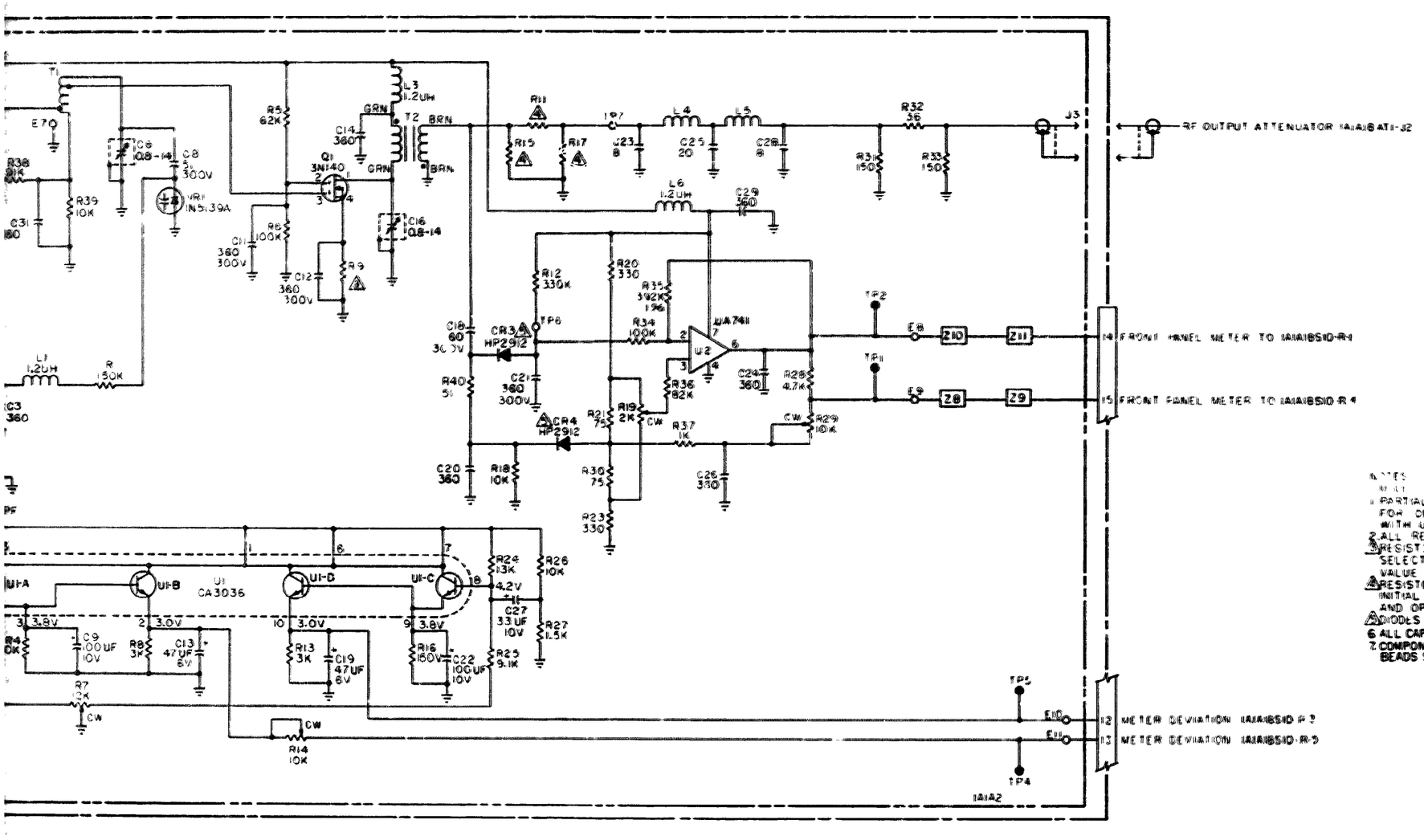



Figure 6-5. Detector output (1A1A2), schematic diagram.

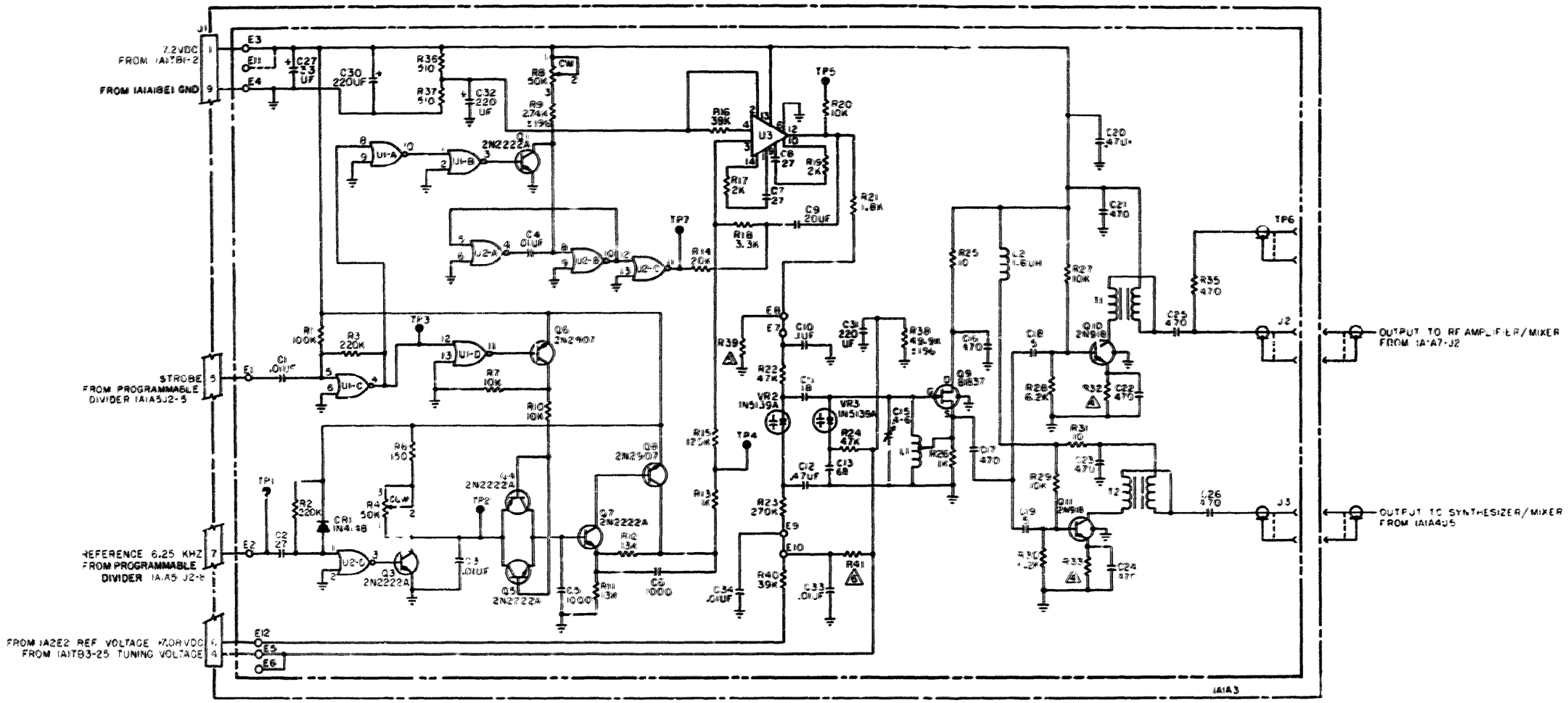
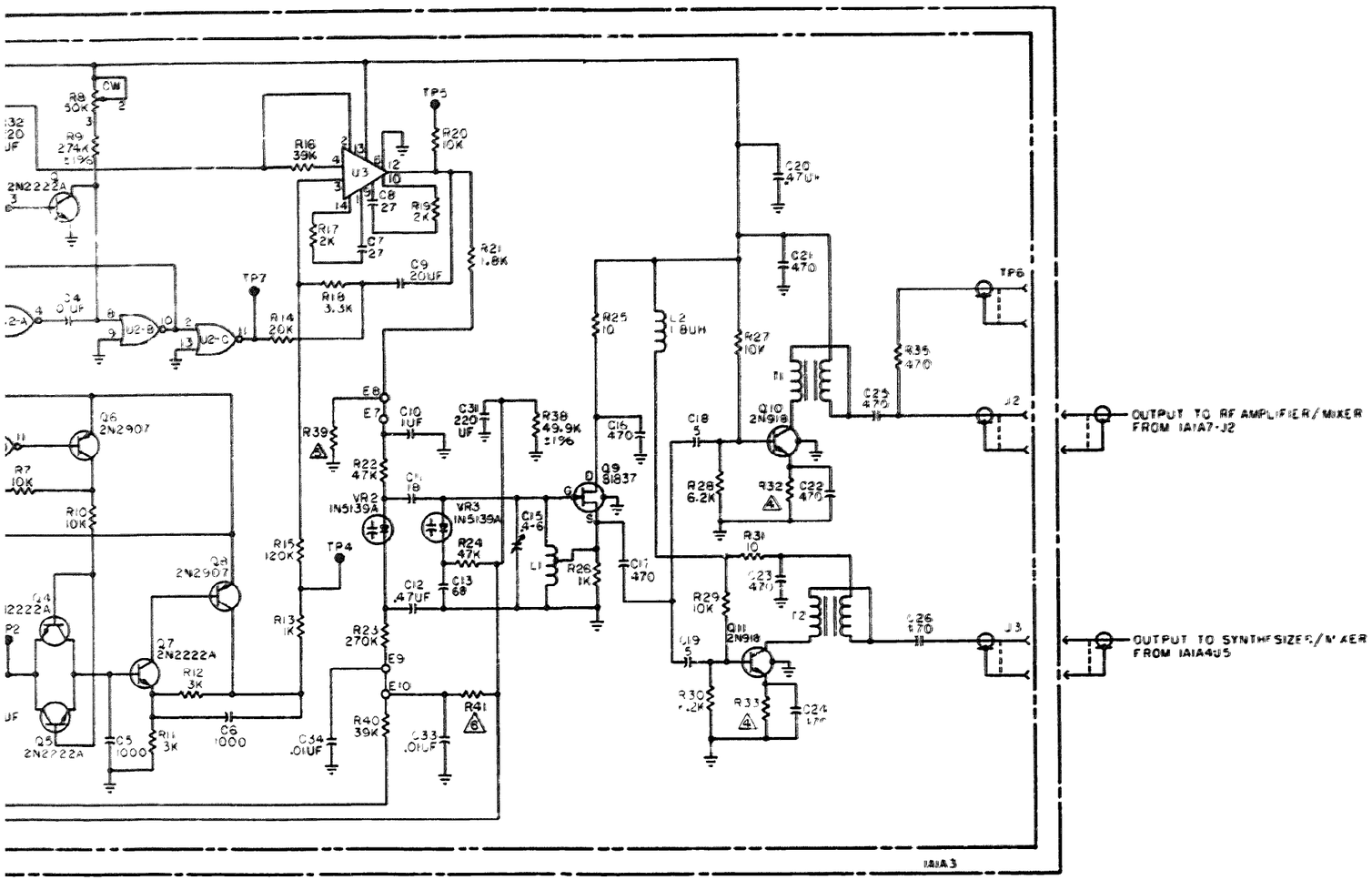



Figure 6-6. Loop filter/VCO (1A1A3), schematic diagram.




NOTES:
UNLESS OTHERWISE SPECIFIED
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE REFERENCE DESIGNATION PREFIX WITH UNIT NO. AND SUB/ASSY DESIGNATION 1A1A3
2. ALL RESISTOR VALUES ARE IN OHMS, 1/8W, ±5%
3. ALL CAPACITANCE VALUES ARE IN PICOFARADS
4. SELECT IN TEST NOMINAL VALUE 470 OHMS APPROVED VALUES AS FOLLOWS: 470, 510, 560, 620, OR 680
5. R39 TO BE SELECTED IN TEST RANGE OF VALUES 4.7K TO 10K
6. R41 TO BE SELECTED IN TEST RANGE OF VALUES 220K TO 1.5MEG
7. INTEGRATED CIRCUITS ARE CD4001AD
8. PIN 7 OF U1 AND U2 IS GROUND AND PIN 14 IS +7.2VDC
9. U3 IS A CA3037

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Figure 6-6. Loop filter/VCO (1A1A3), schematic diagram.

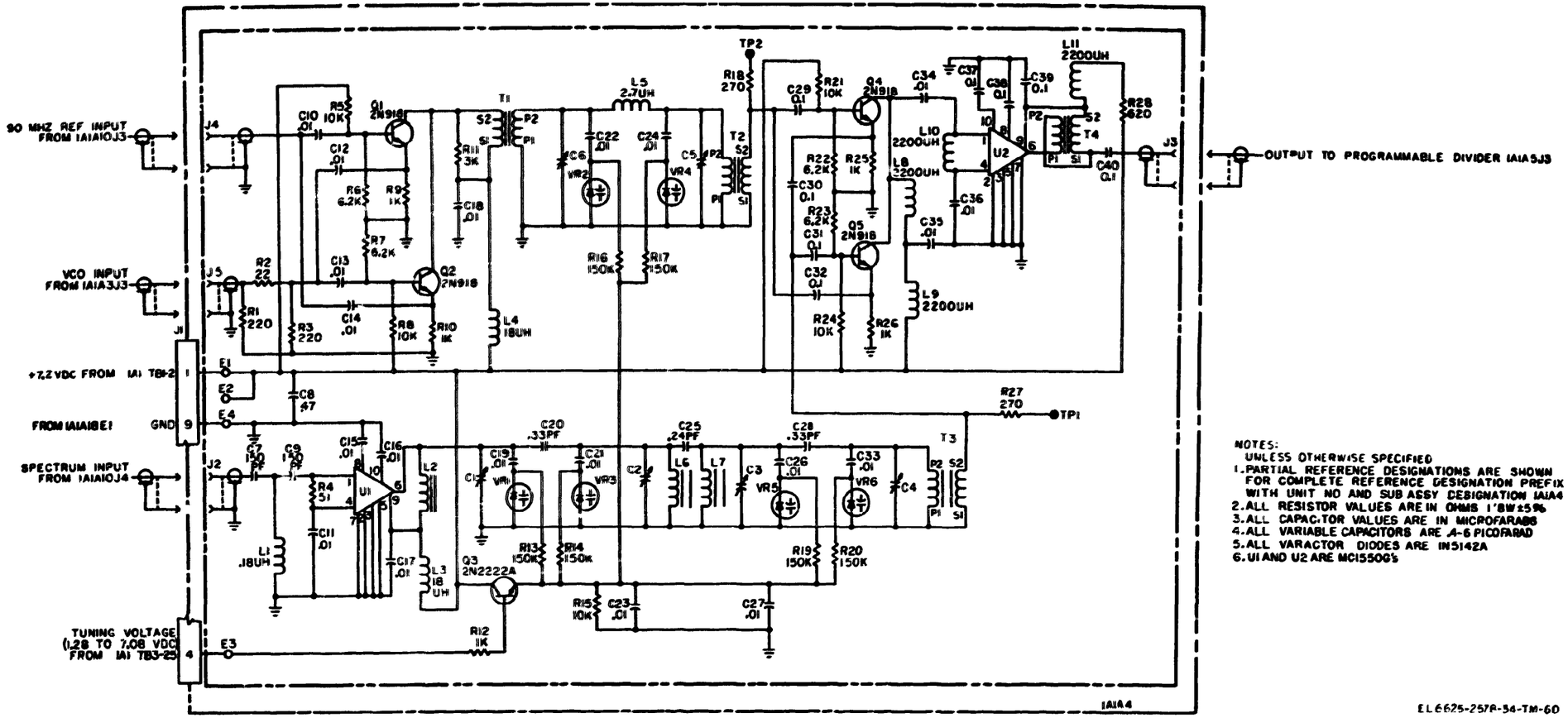



Figure 6-7. Synthesizer mixer (1A1A4), schematic diagram.

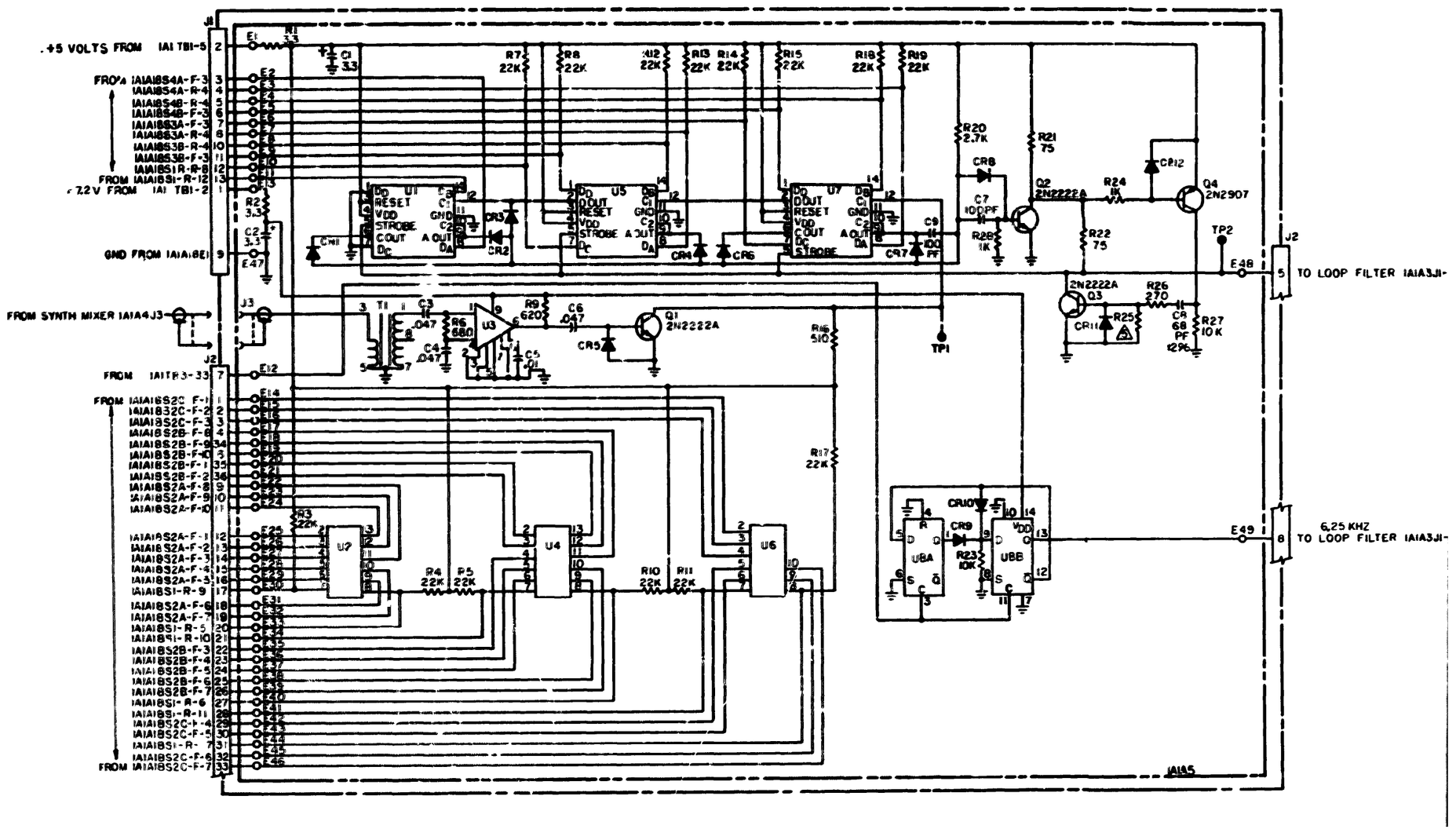
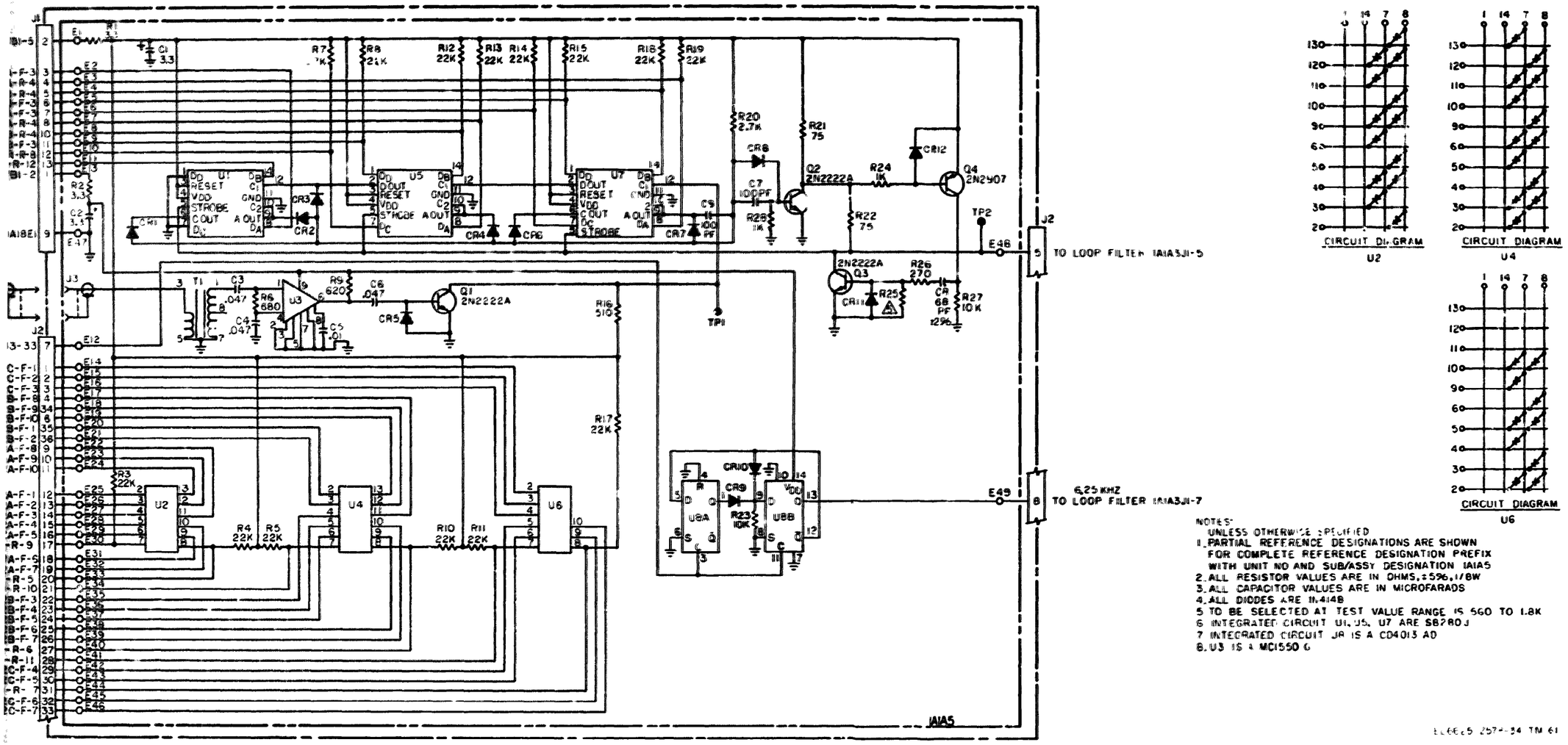



Figure 6-8. Programmable divider (1A1A5), schematic diagram.













NOTES:
UNLESS OTHERWISE SPECIFIED
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE REFERENCE DESIGNATION PREFIX WITH UNIT NO AND SUB/ASSY DESIGNATION 1A1A5
2. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/8W
3. ALL CAPACITOR VALUES ARE IN MICROFARADS
4. ALL DIODES ARE 1N4148
5 TO BE SELECTED AT TEST VALUE RANGE IS 560 TO 1.8K
6 INTEGRATED CIRCUIT U1, U5, U7 ARE SB2803
7 INTEGRATED CIRCUIT U8 IS A CD4013 AD
8. U3 IS A MC1550 G

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Figure 6-8. Programmable divider (1A1A5), schematic diagram.

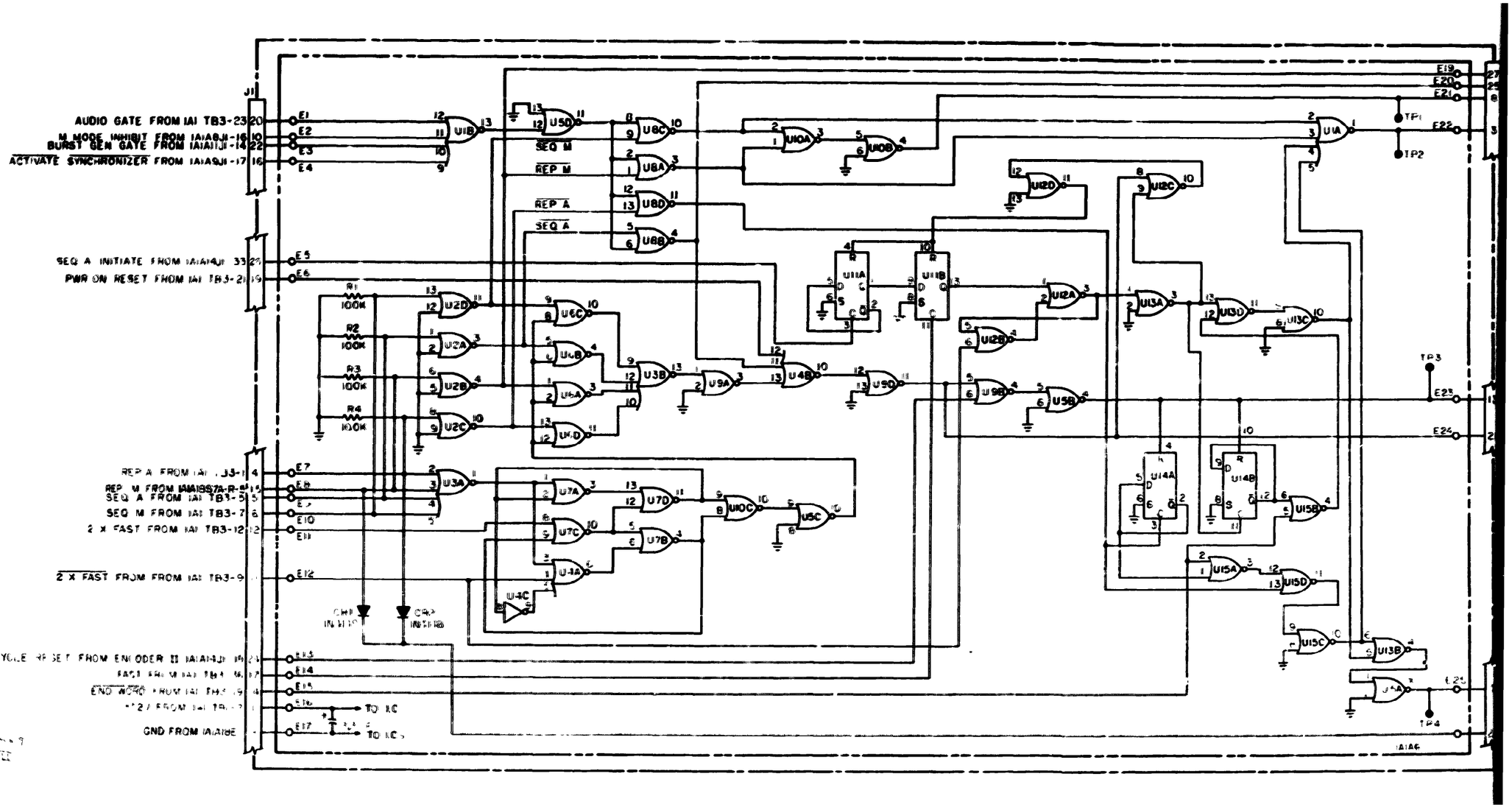



Figure 6-9. Mode control I (1A1A6), schematic diagram.

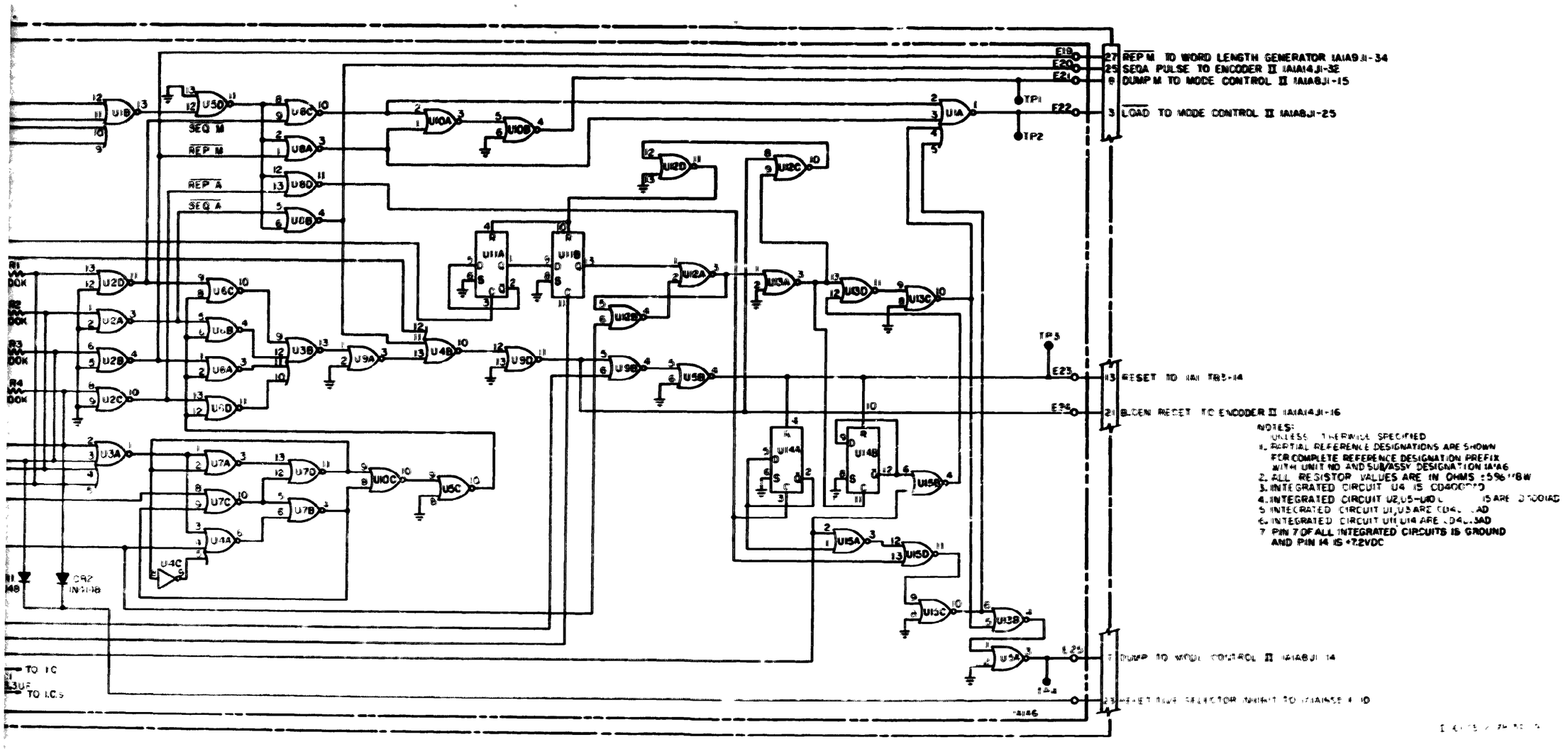



Figure 6-9. Mode control I (1A1A6), schematic diagram.

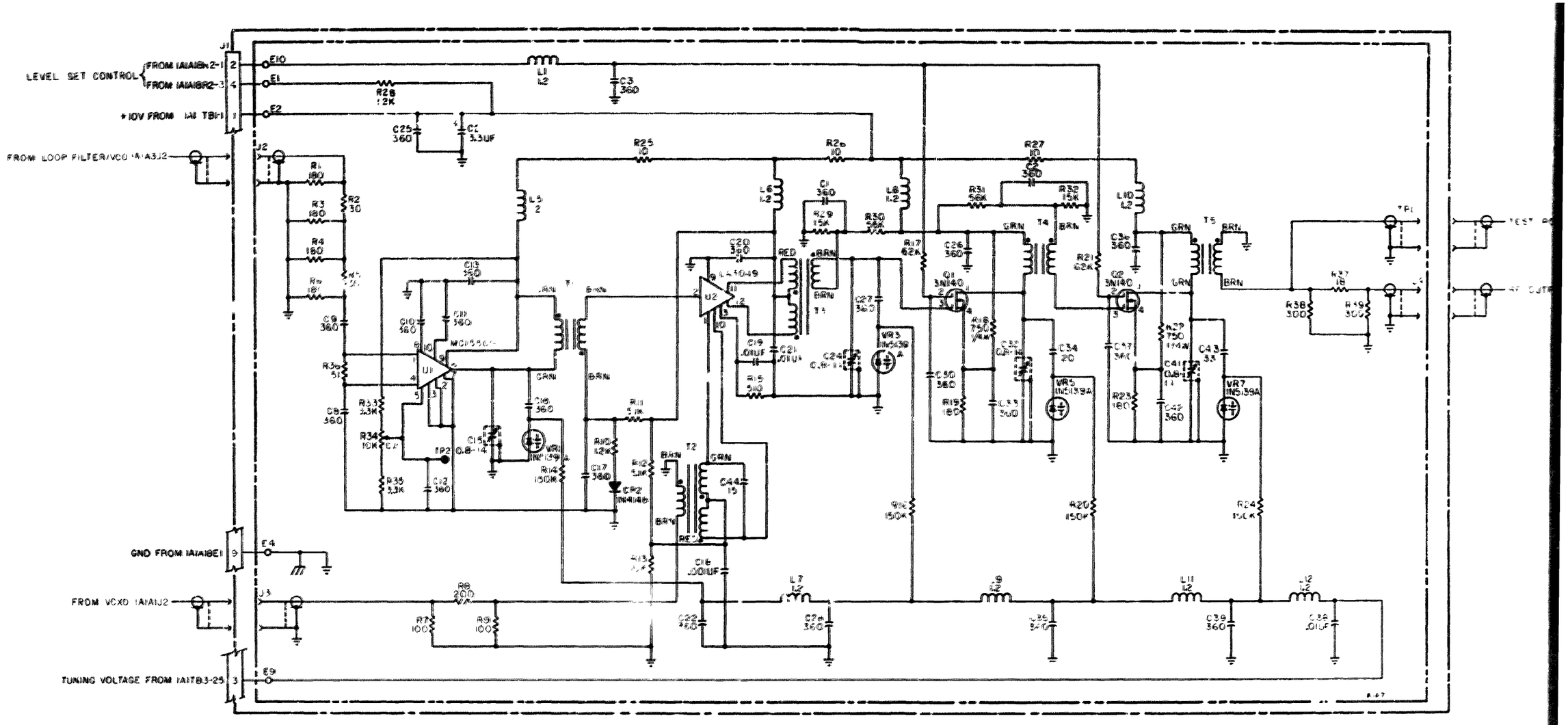
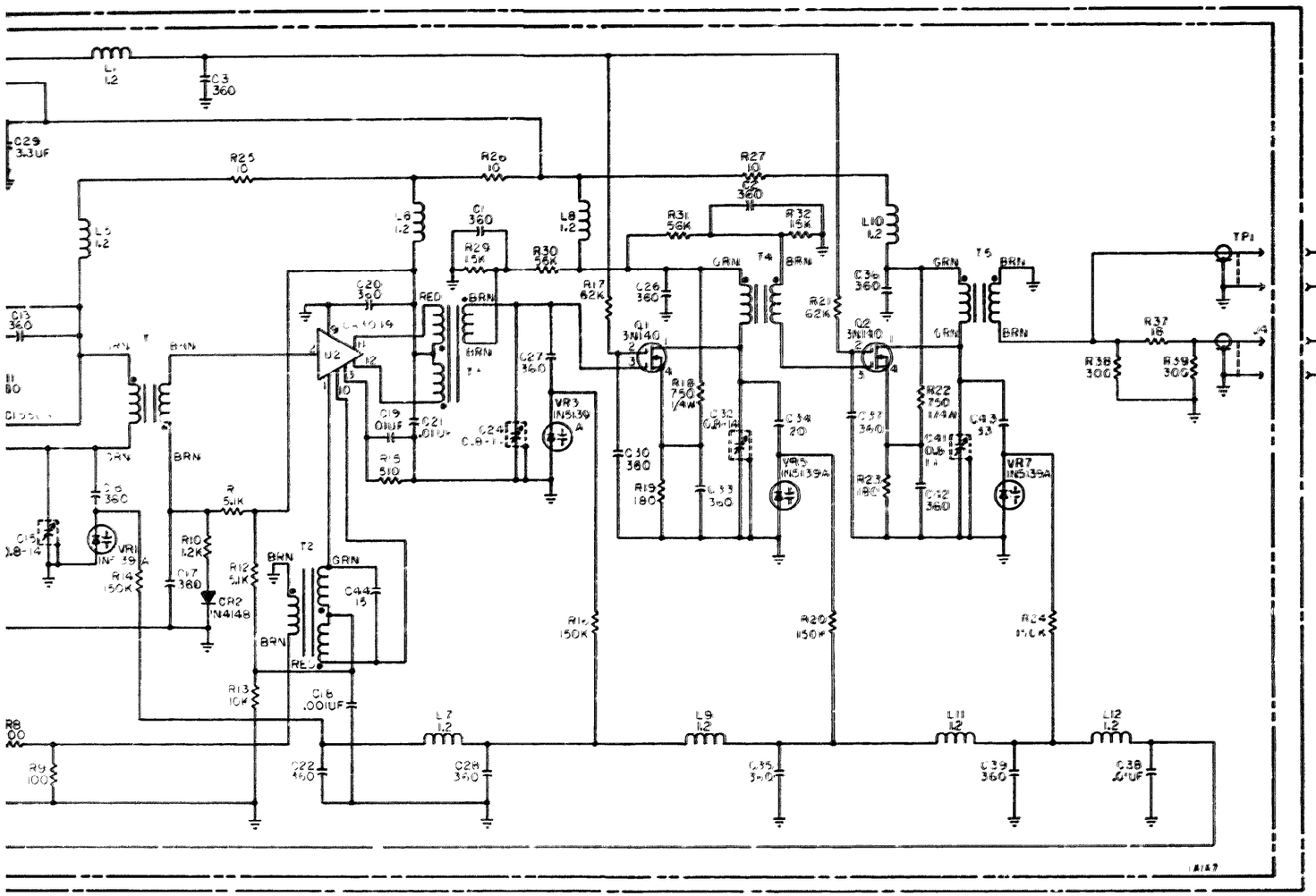



Figure 6-10. Rf mixer amplifier (1A1A7), schematic diagram.




NOTES
UNLESS OTHERWISE SPECIFIED
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE REFERENCE DESIGNATION PREFIX WITH UNIT NO AND SUB/ASSY DESIGNATION 1A1A7
2. ALL RESISTOR VALUES ARE IN OHMS 1/8W ±5%
3. ALL CAPACITOR VALUES ARE IN PICOFARADS
4. ALL INDUCTOR VALUES ARE IN MICROHENRIES

Figure 6-10. Rf mixer amplifier (1A1A7), schematic diagram.

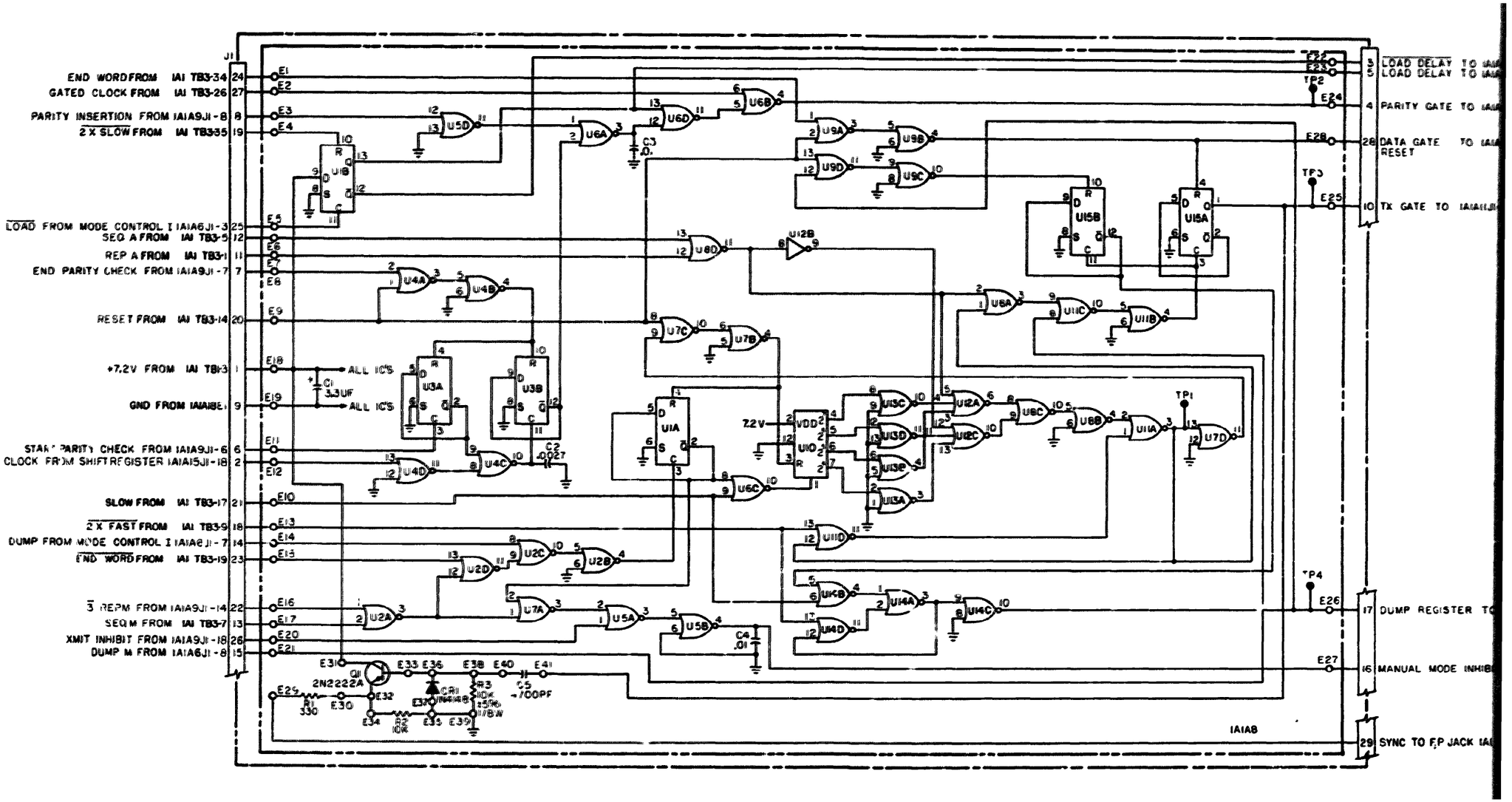
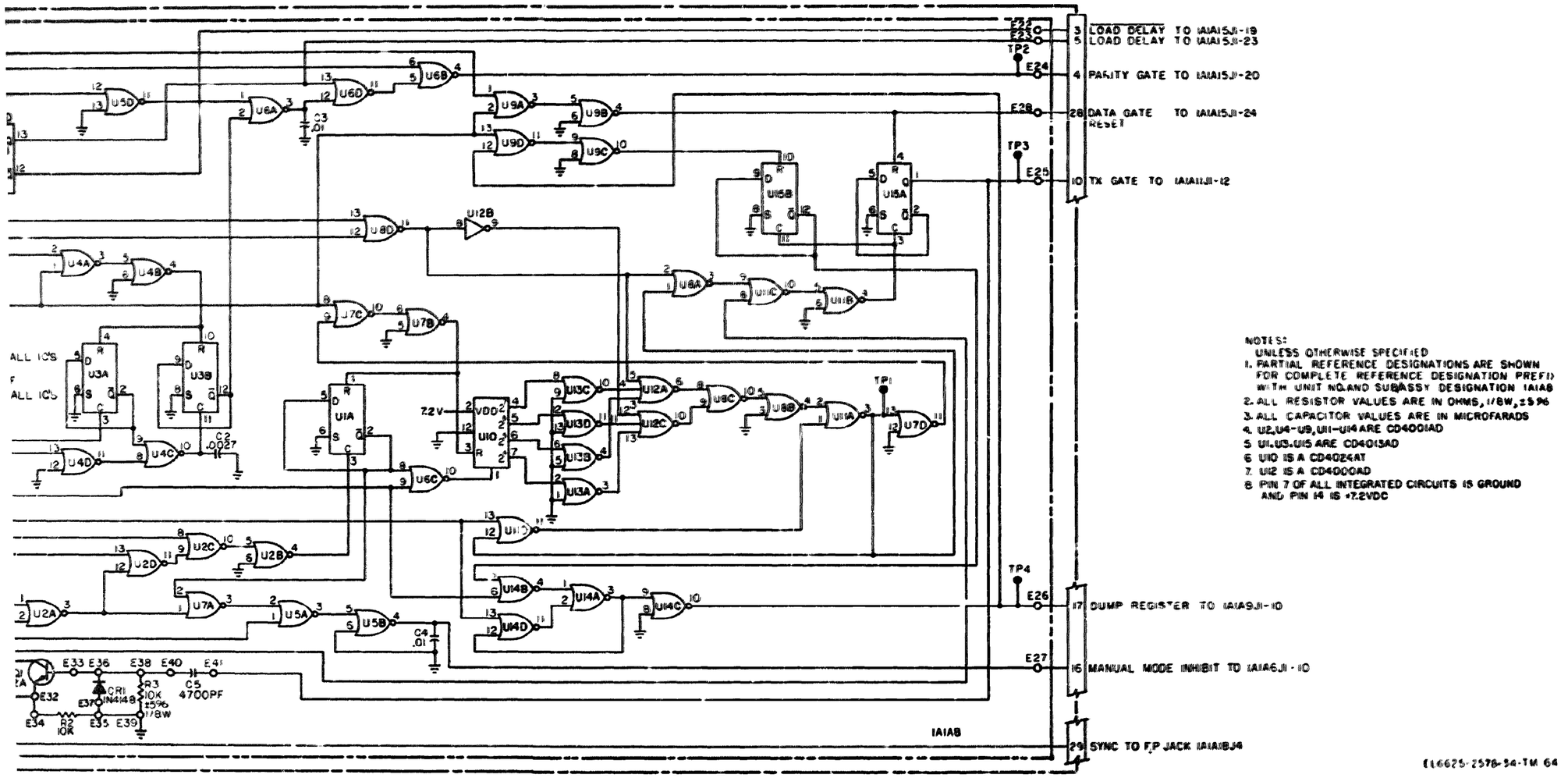



Figure 6-11. Mode control II (1A1A8), schematic diagram.




NOTES:
UNLESS OTHERWISE SPECIFIED
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE REFERENCE DESIGNATION PREFIX WITH UNIT NO. AND SUBASSY DESIGNATION 1A1A8
2. ALL RESISTOR VALUES ARE IN OHMS, 1/8W, ±5%
3. ALL CAPACITOR VALUES ARE IN MICROFARADS
4. U2, U4-U9, U11-U14 ARE CD4001AD
5. U1, U3, U15 ARE CD4013AD
6. U10 IS A CD4024AT
7. U12 IS A CD4000AD
8. PIN 7 OF ALL INTEGRATED CIRCUITS IS GROUND AND PIN 14 IS +7.2VDC

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Figure 6-11. Mode control II (1A1A8), schematic diagram.

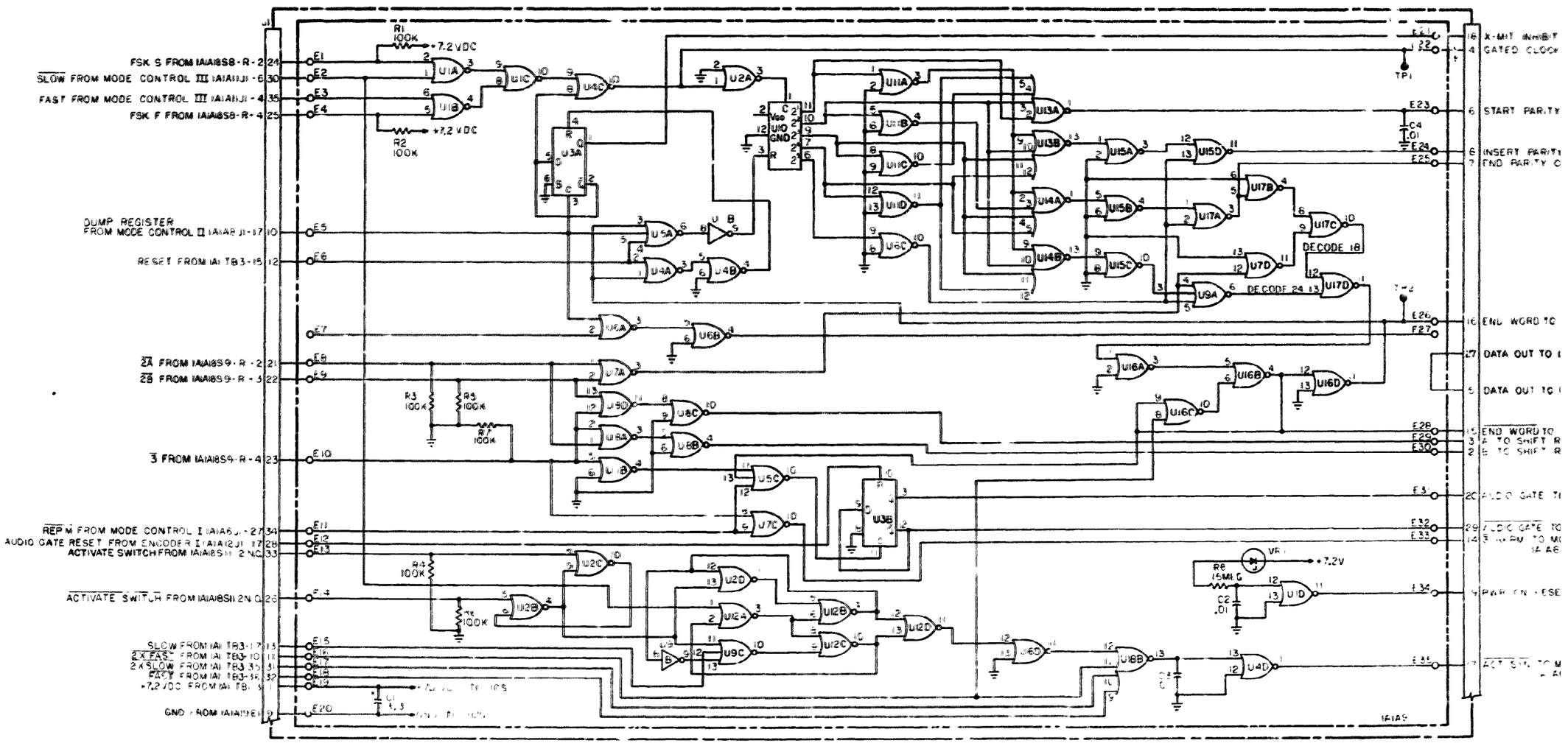
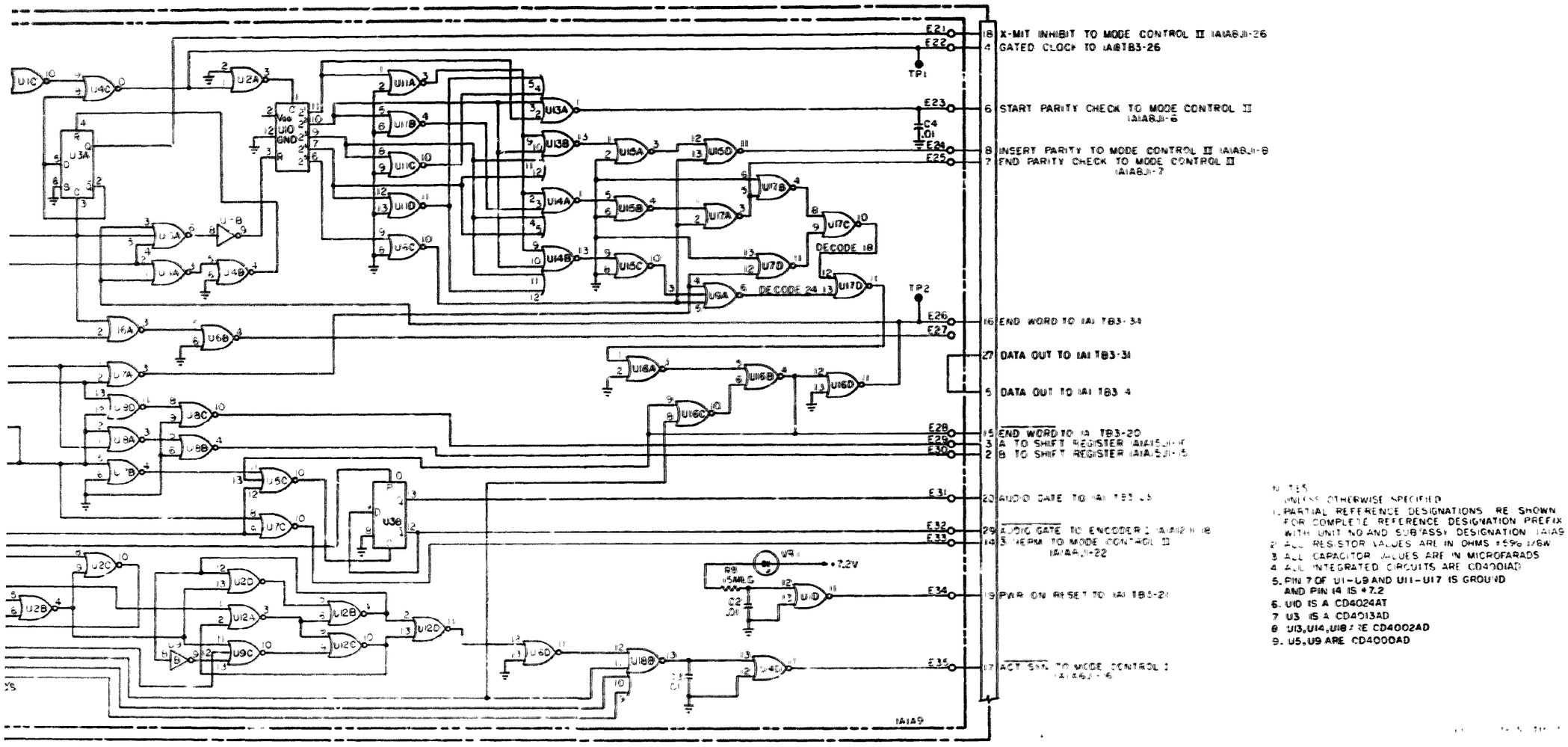



Figure 6-12. Word length generator (1A1A9), schematic diagram.




NOTES
UNLESS OTHERWISE SPECIFIED
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE REFERENCE DESIGNATION PREFIX WITH UNIT NO AND SUBASSY DESIGNATION (A1A9)
2. ALL RESISTOR VALUES ARE IN OHMS ±5% 1/8W
3. ALL CAPACITOR VALUES ARE IN MICROFARADS
4. ALL INTEGRATED CIRCUITS ARE CD4030AD
5. PIN 7 OF U1-U8 AND U11-U17 IS GROUND AND PIN 14 IS +7.2
6. U10 IS A CD4024AT
7. U3 IS A CD4013AD
8. U13, U14, U18 ARE CD4002AD
9. U5, U9 ARE CD4000AD

Figure 6-12. Word length generator (1A1A9), schematic diagram.

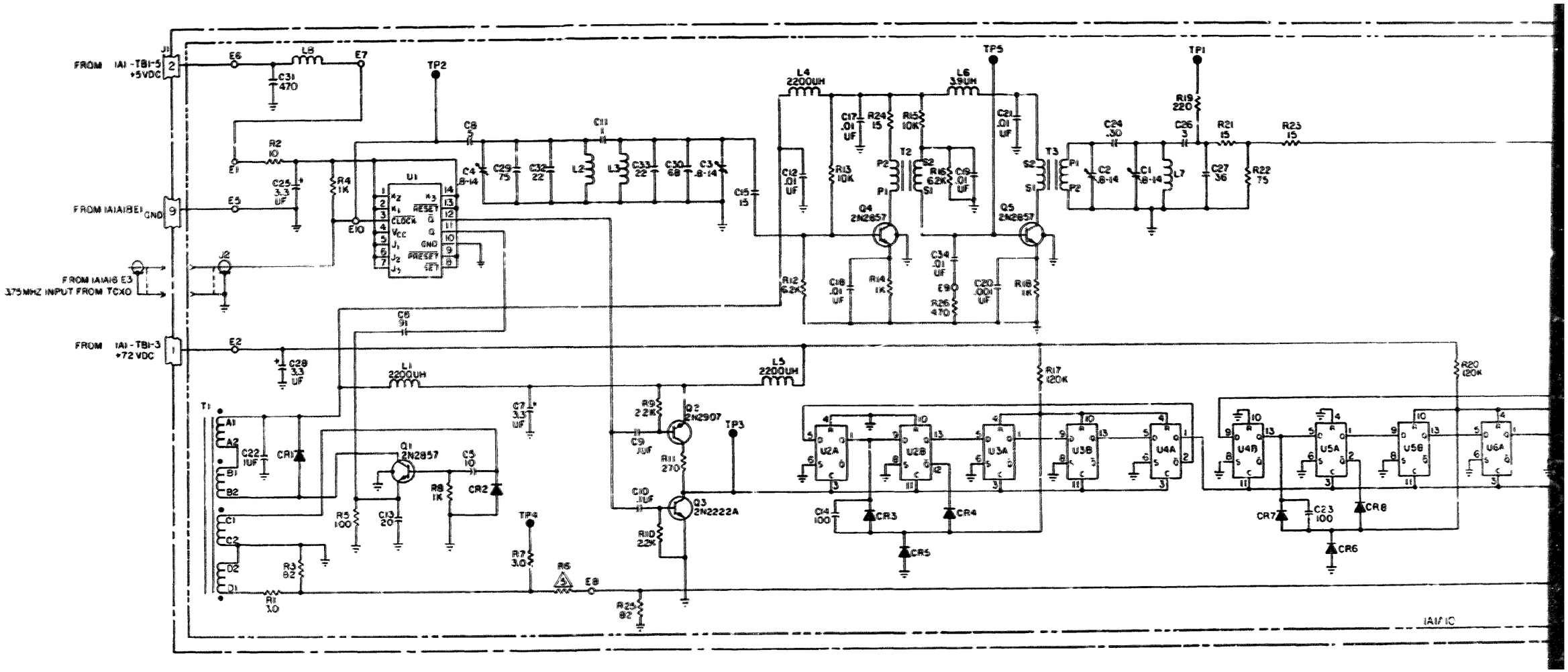



Figure 6-13. Reference generator (1A1A10), schematic diagram.

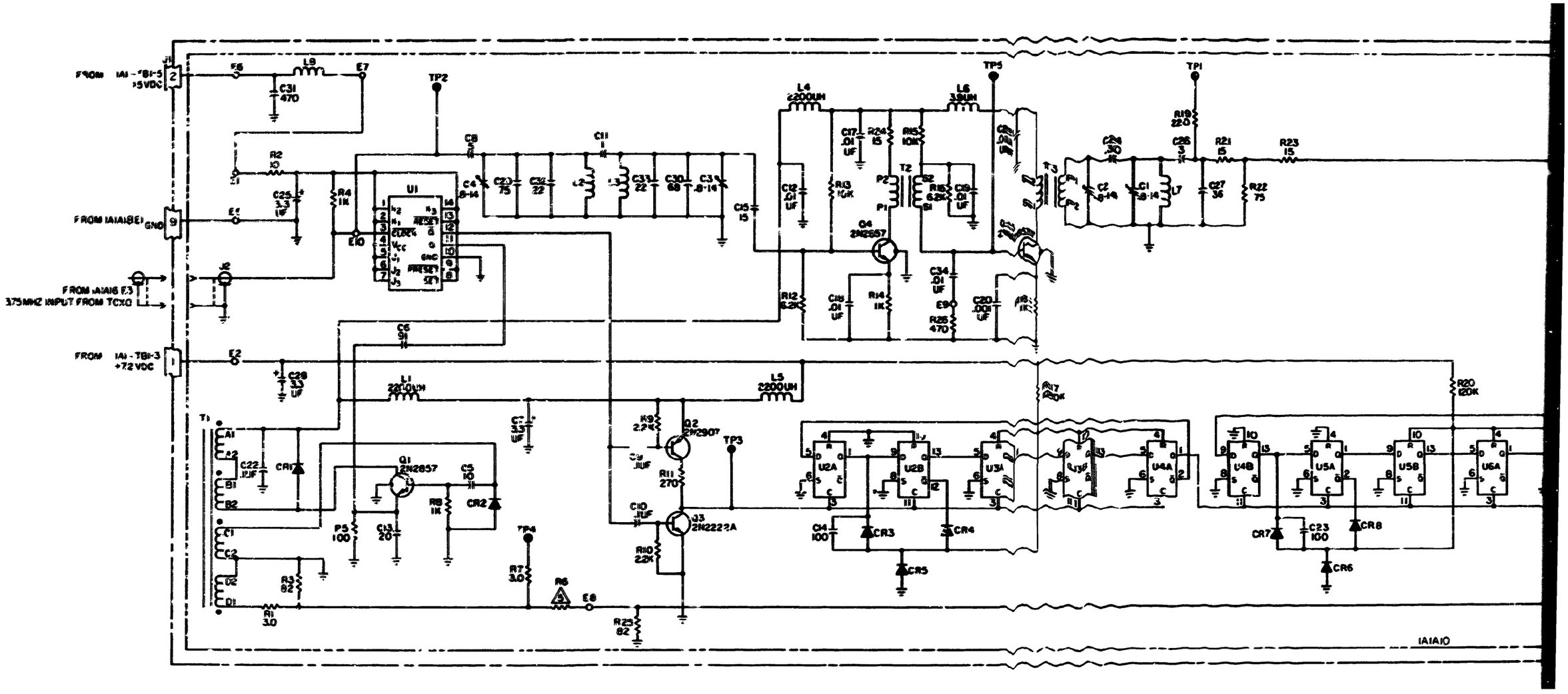
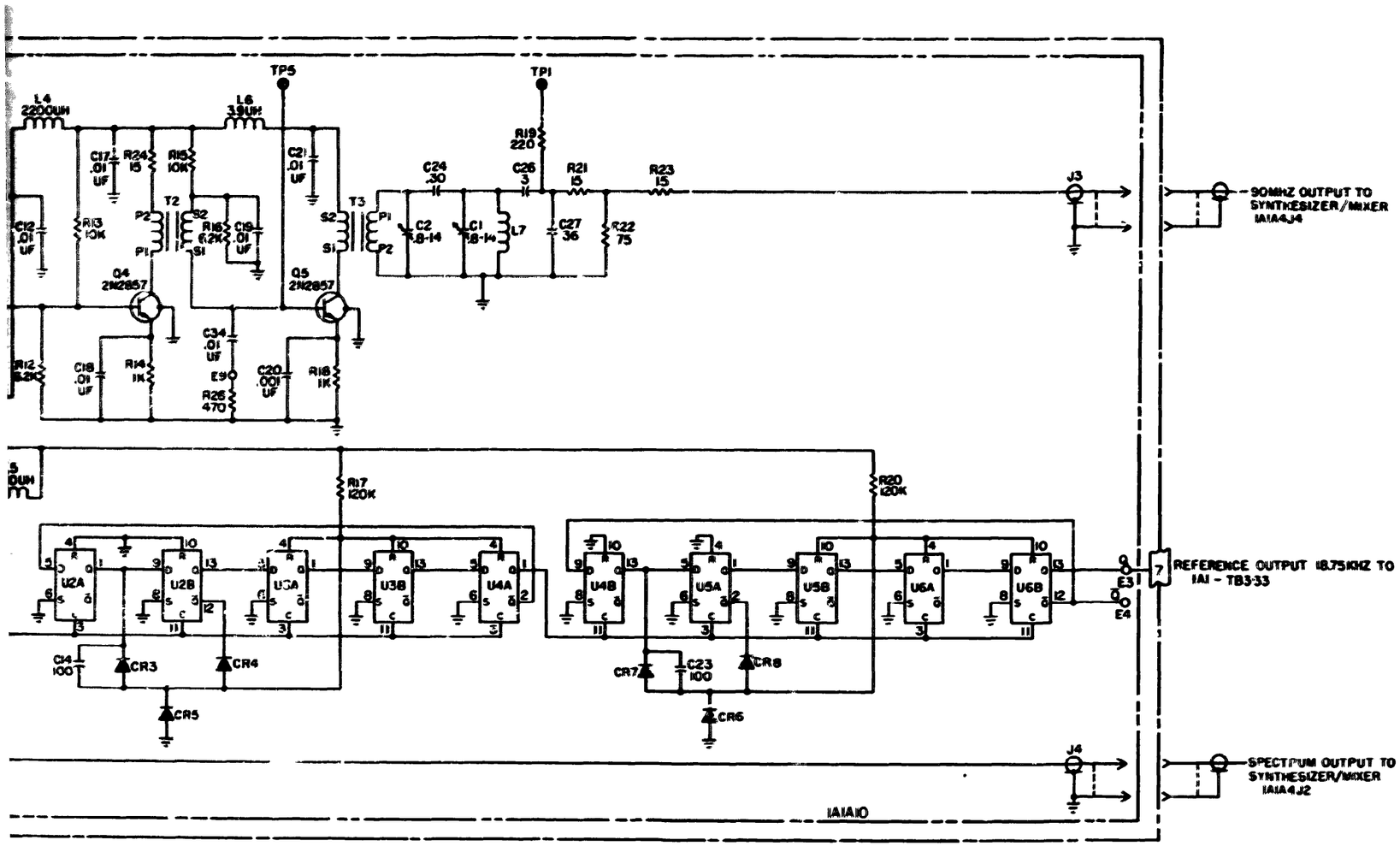



Figure 6-13. Reference generator (1A1A10), schematic diagram.




NOTES:
UNLESS OTHERWISE SPECIFIED
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE REFERENCE DESIGNATION PREFIX WITH UNIT NUMBER AND SUB/ASSY DESIGNATION 1A1A10
2. ALL RESISTOR VALUES ARE IN OHMS 1/8W ±5%
3. ALL DIODES ARE IN4148
4. ALL CAPACITOR VALUES ARE IN PICOFARADS.
5. R6 TO BE SELECTED IN TEST: RANGE OF VALUES FROM 91 TO 150.
6. INTEGRATED CIRCUITS U2-U6 ARE CD4013AD.
7. PIN 7 OF U2-U6 IS GROUND.
8. PIN 14 OF U2-U6 IS +7.2VDC

Figure 6-13. Reference generator (1A1A10), schematic diagram.

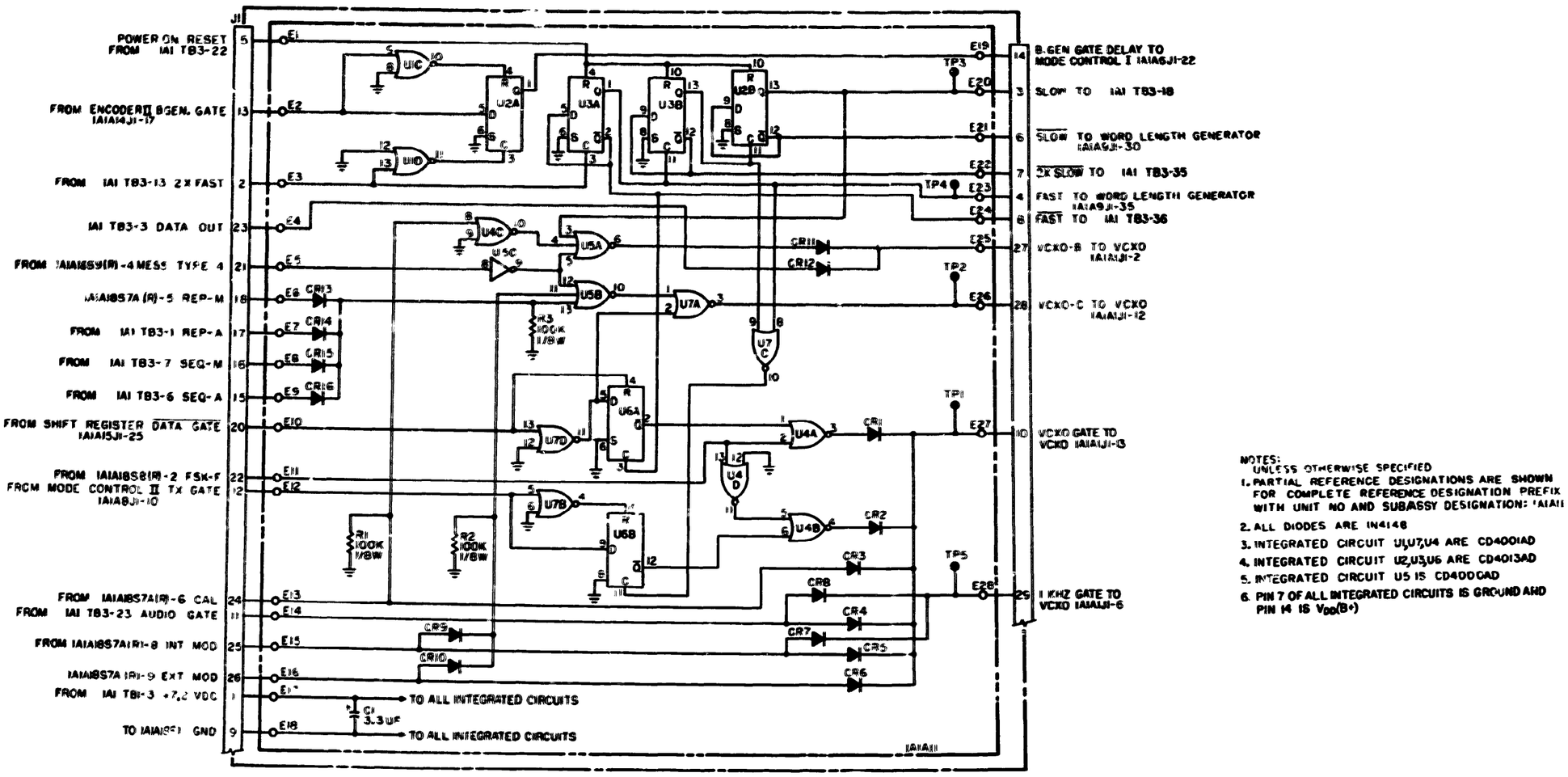



Figure 6-14. Mode control III (1A1A11), schematic diagram.

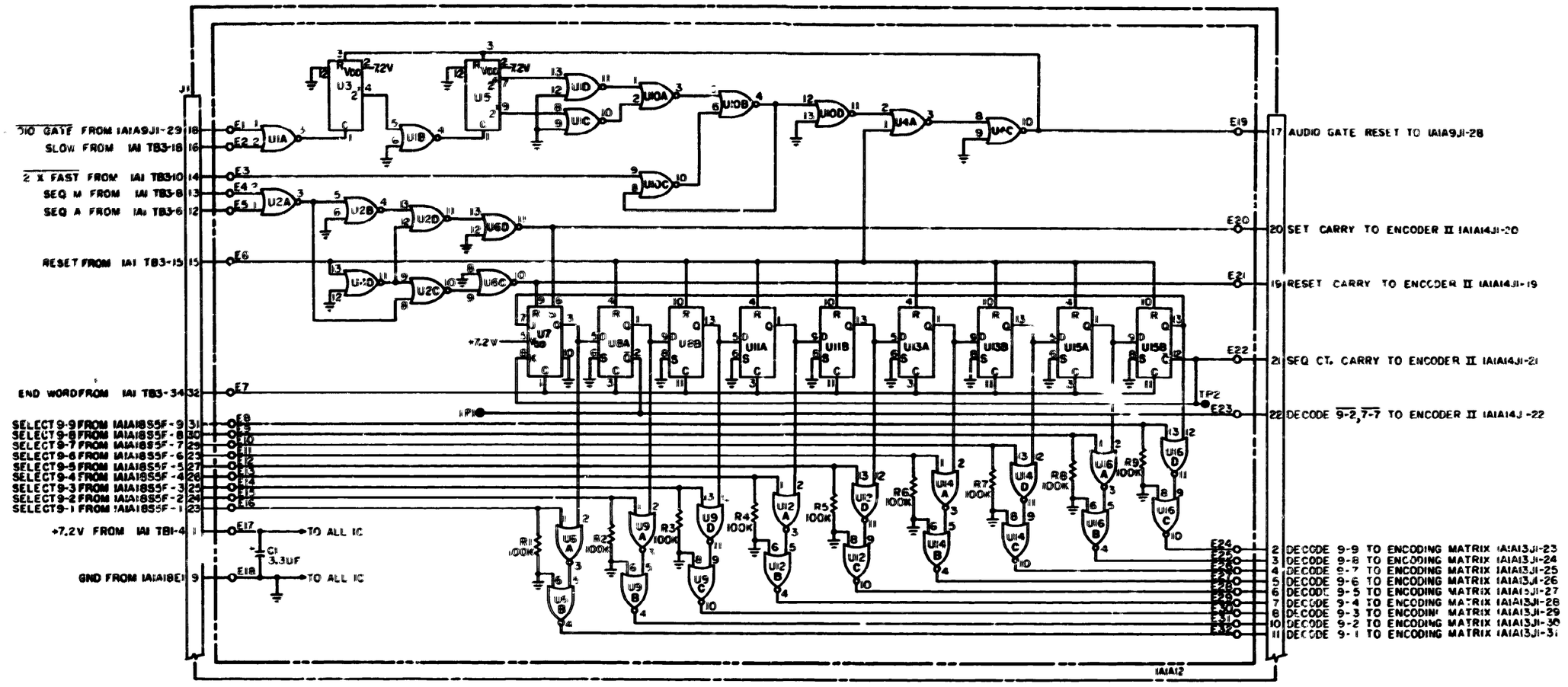
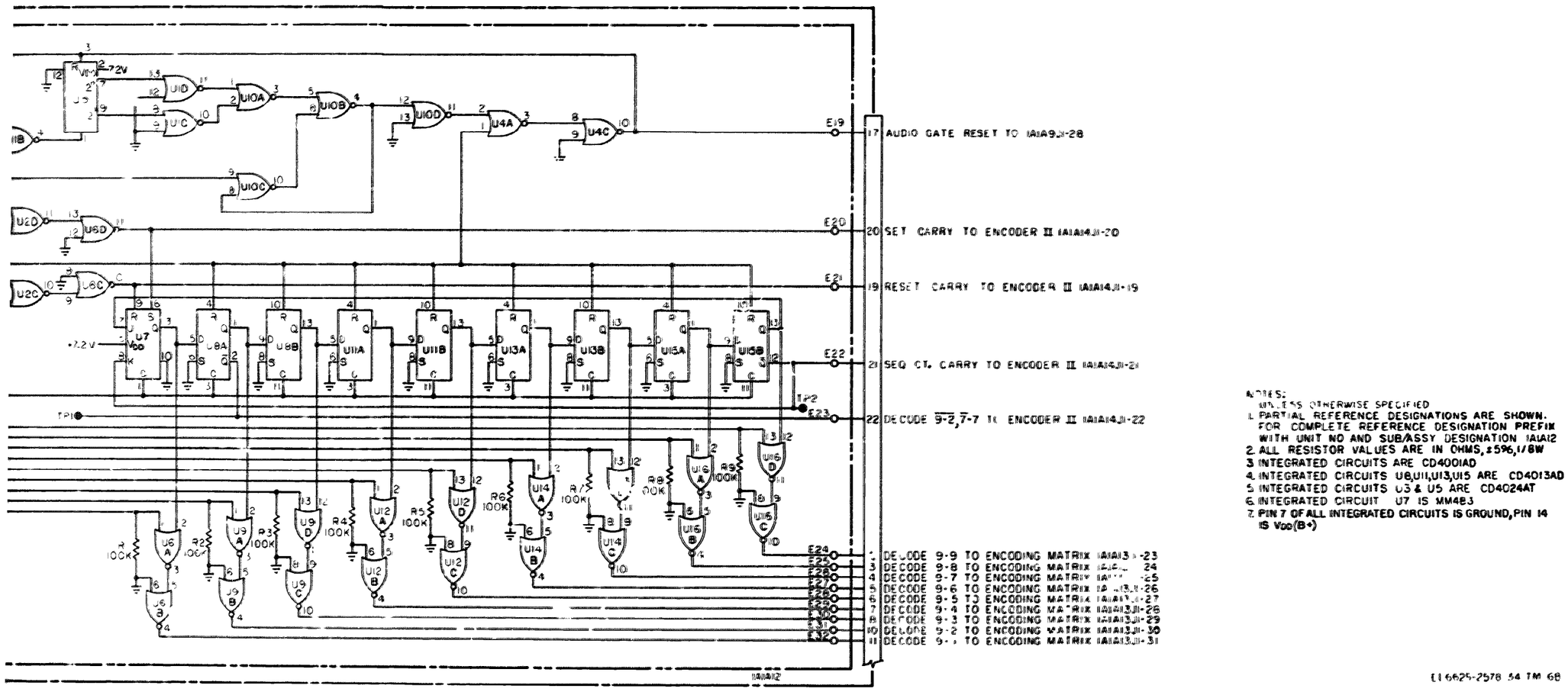



Figure 6-15. Encoder I (1A1A12), schematic diagram.




NOTES:
UNLESS OTHERWISE SPECIFIED
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE REFERENCE DESIGNATION PREFIX WITH UNIT NO AND SUB/ASSY DESIGNATION 1A1A12
2. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/8W
3. INTEGRATED CIRCUITS ARE CD4001AD
4. INTEGRATED CIRCUITS U8,U11,U13,U15 ARE CD4013AD
5. INTEGRATED CIRCUITS U3 & U5 ARE CD4024AT
6. INTEGRATED CIRCUIT U7 IS MM483
7. PIN 7 OF ALL INTEGRATED CIRCUITS IS GROUND, PIN 14 IS $V_{DD}$(B+)

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Figure 6-15. Encoder I (1A1A12), schematic diagram.

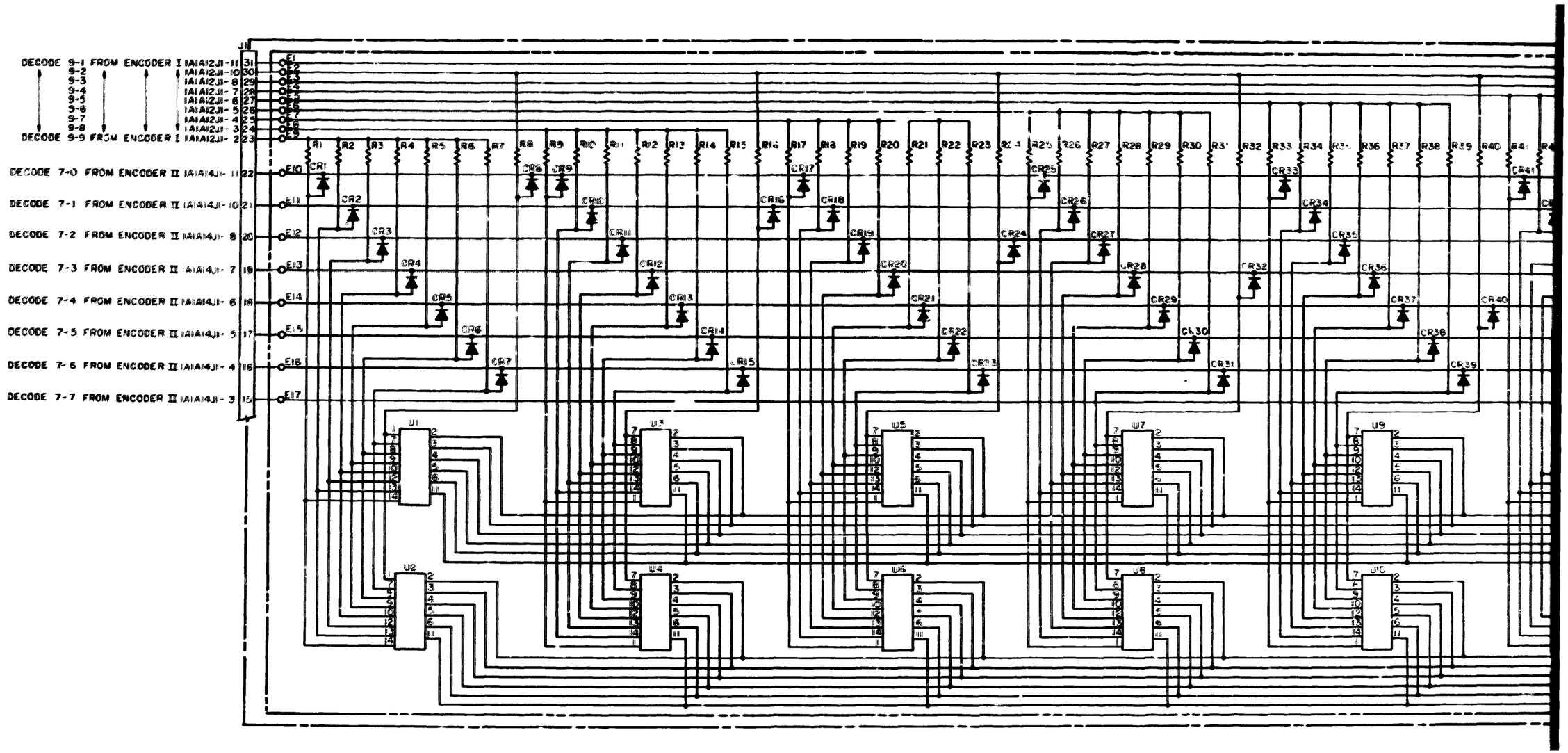



Figure 6-16(1). Encoder matrix (1A1A13), schematic diagram (sheet 1 of 2).

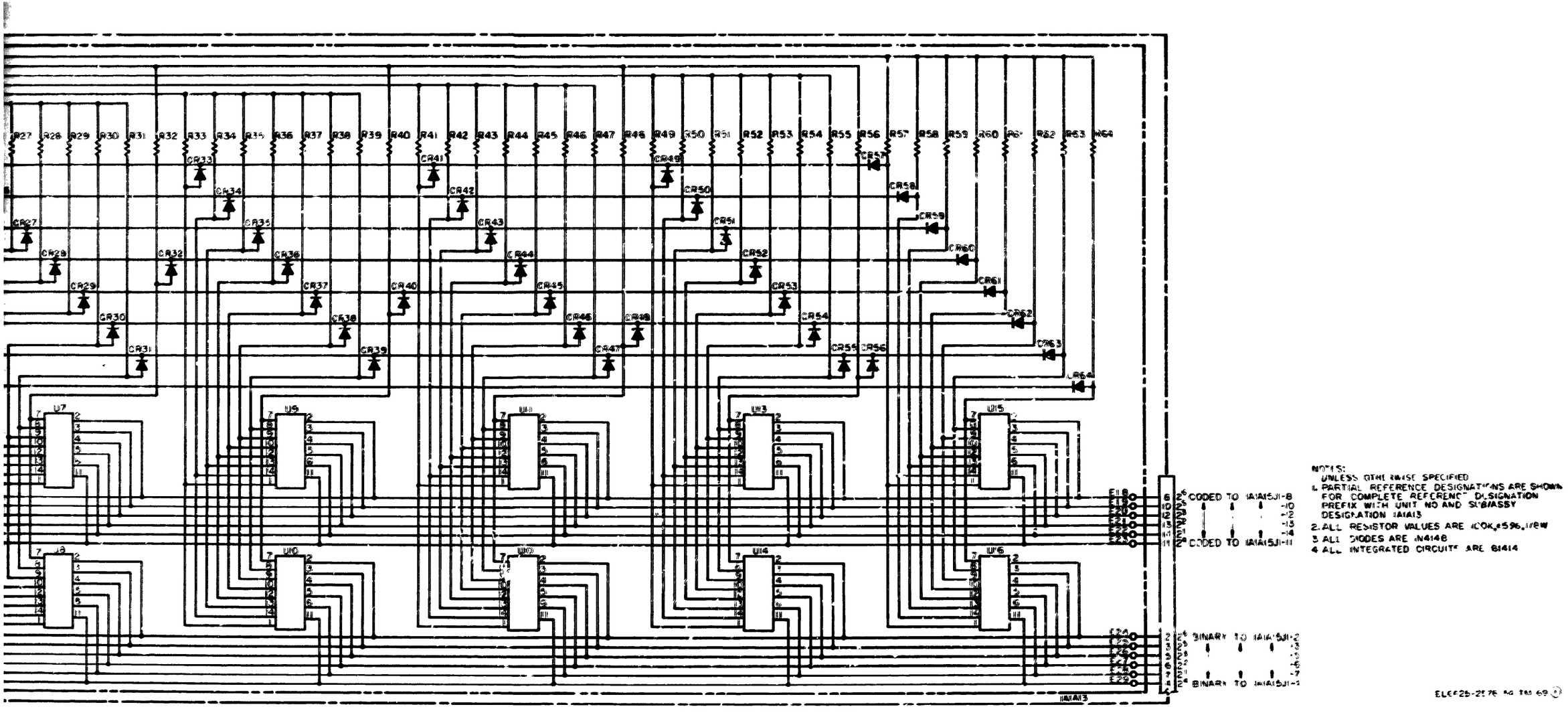
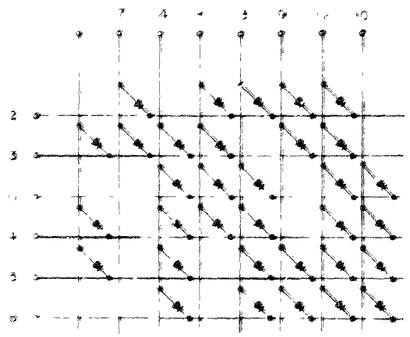
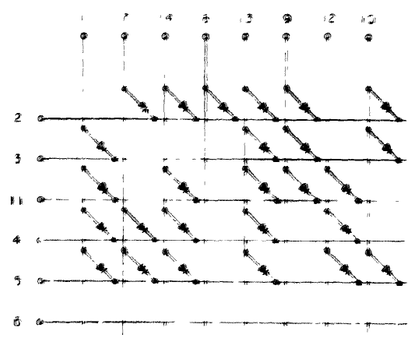
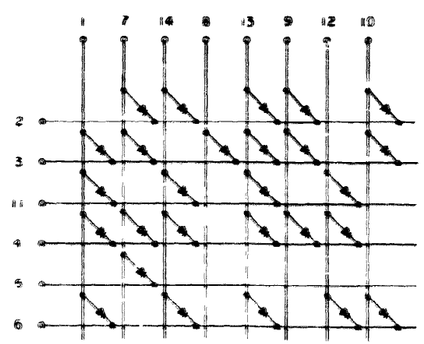
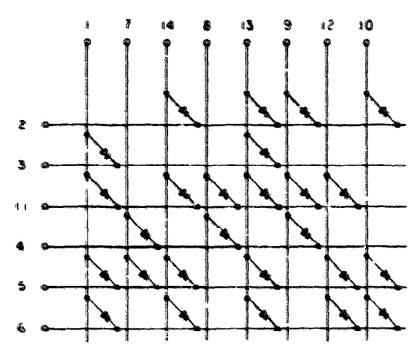


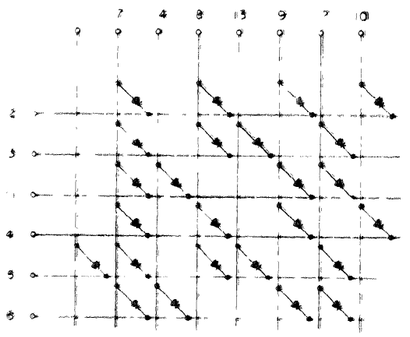

Figure 6-16(1). Encoder matrix (1A1A13), schematic diagram (sheet 1 of 2).

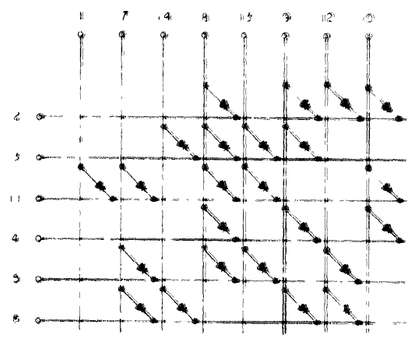


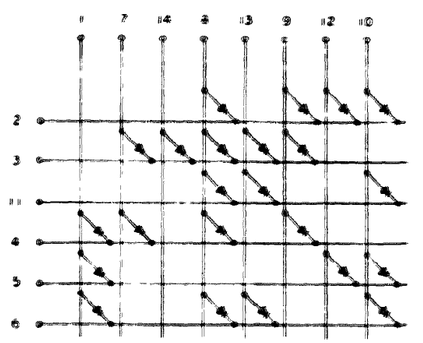



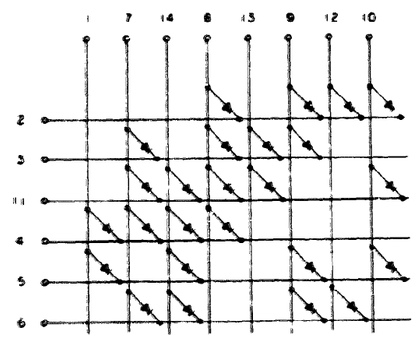




Figure 6-16(2). Encoder matrix (1A1A13), schematic diagram (sheet 2 of 2).

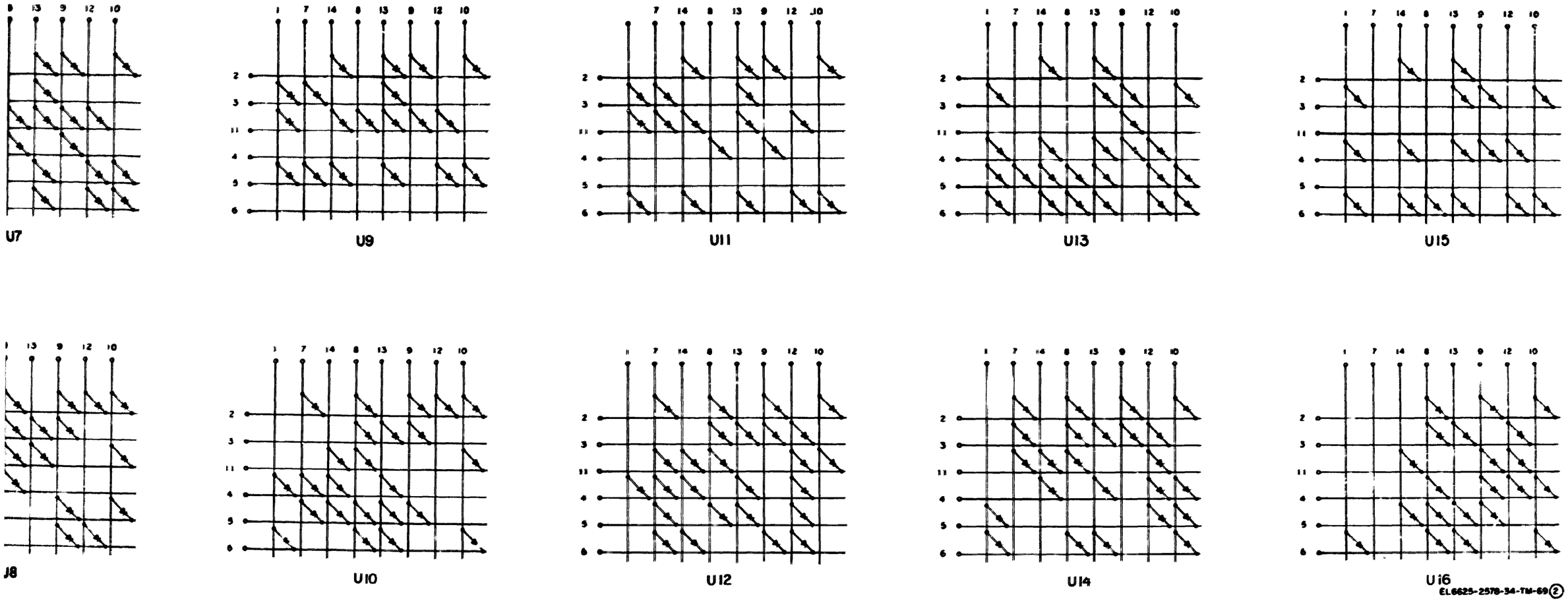



Figure 6-16(2). Encoder matrix (1A1A13), schematic diagram (sheet 2 of 2).

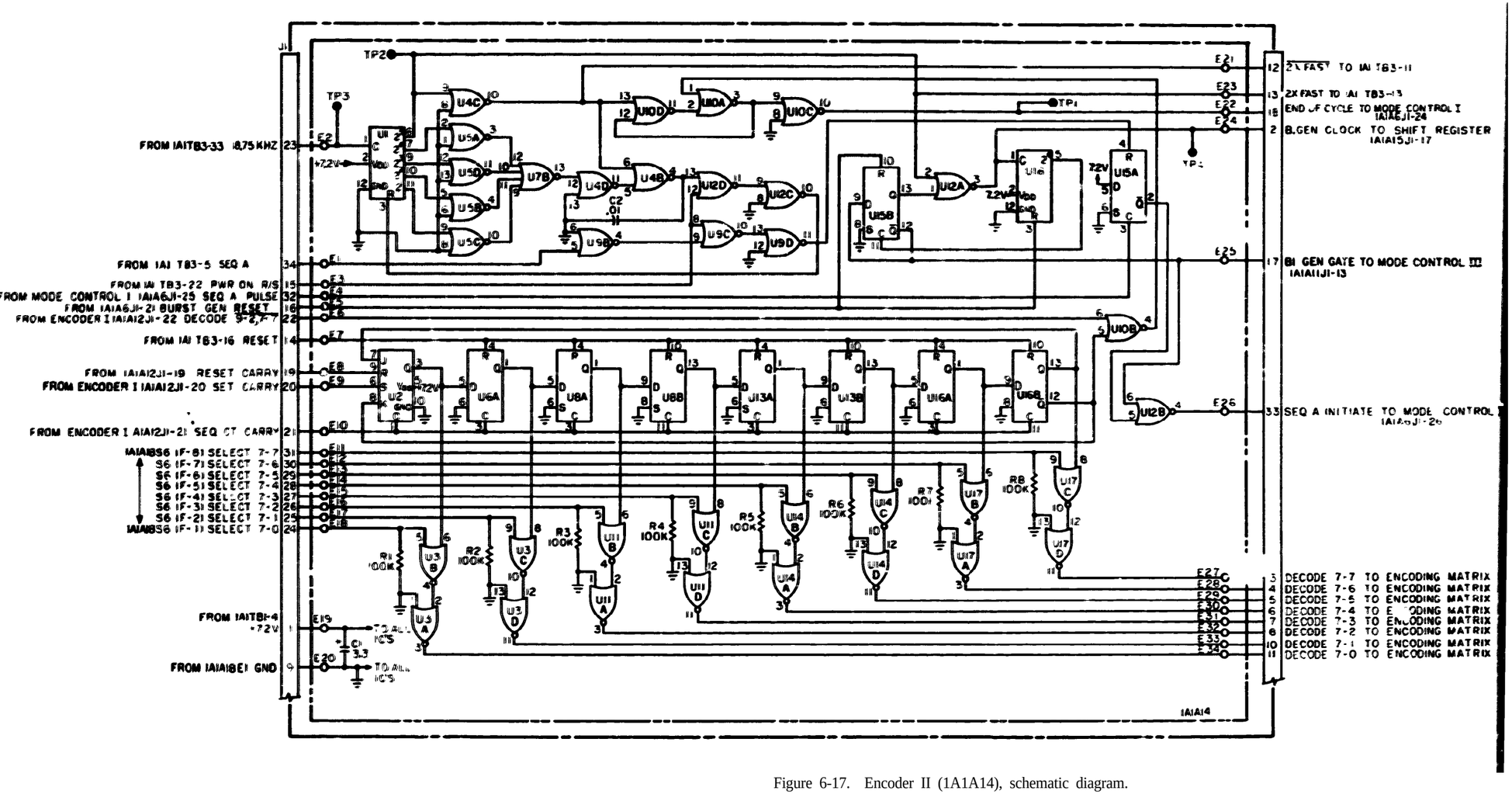



Figure 6-17. Encoder II (1A1A14), schematic diagram.

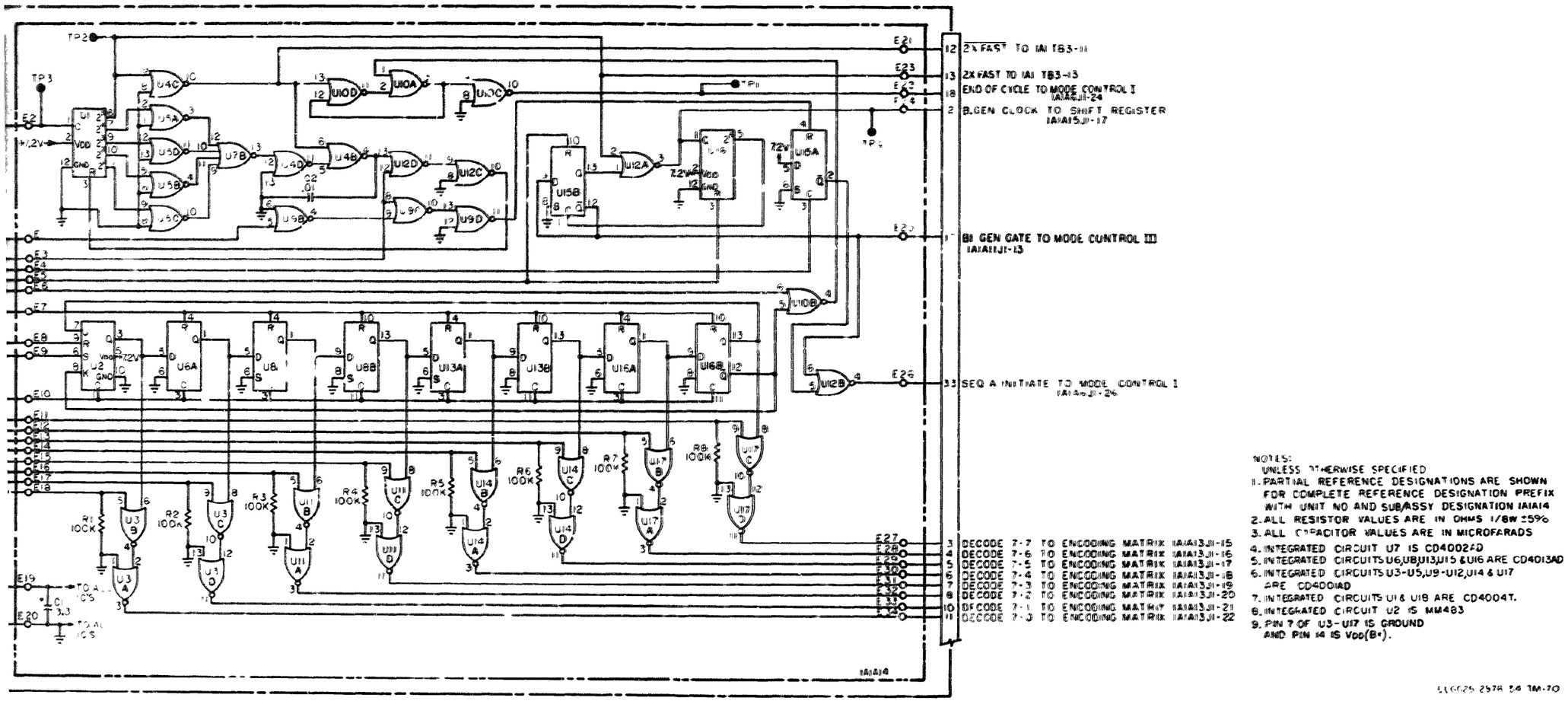



Figure 6-17. Encoder II (1A1A14), schematic diagram.

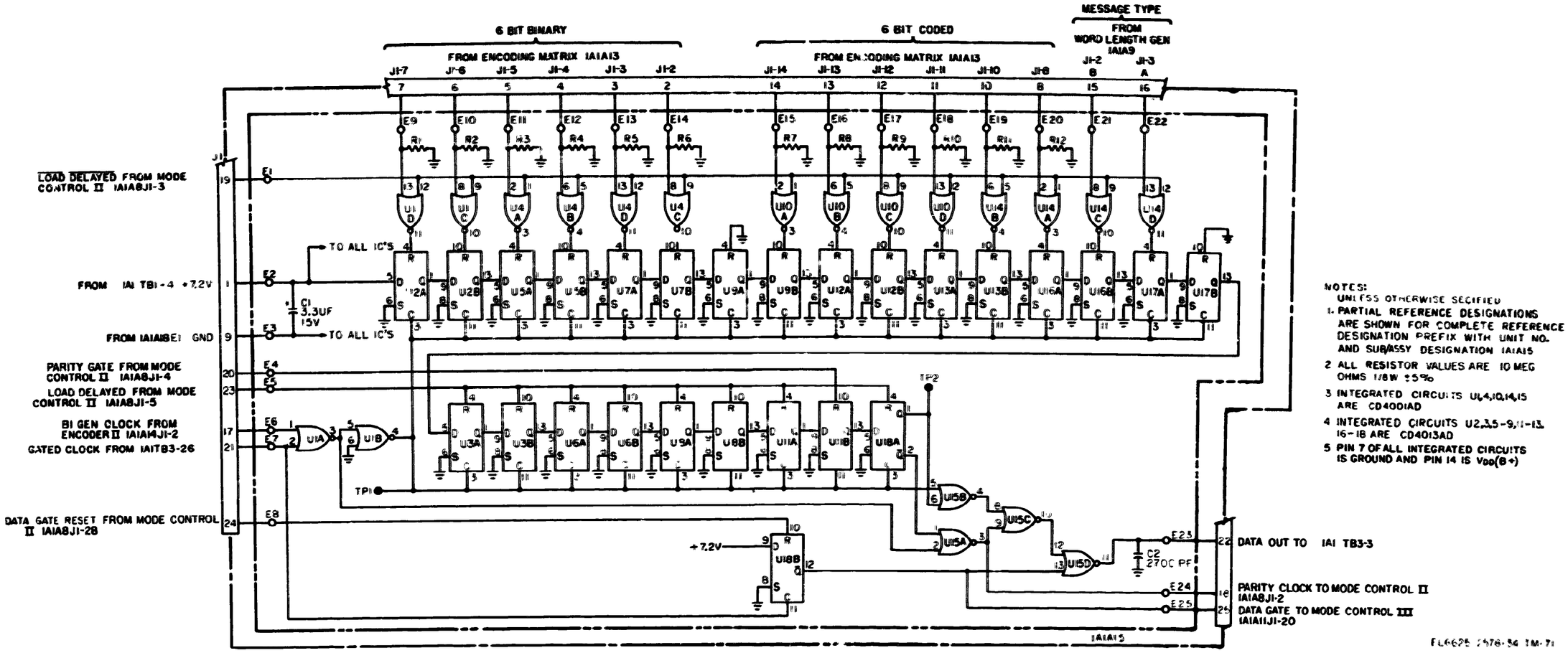
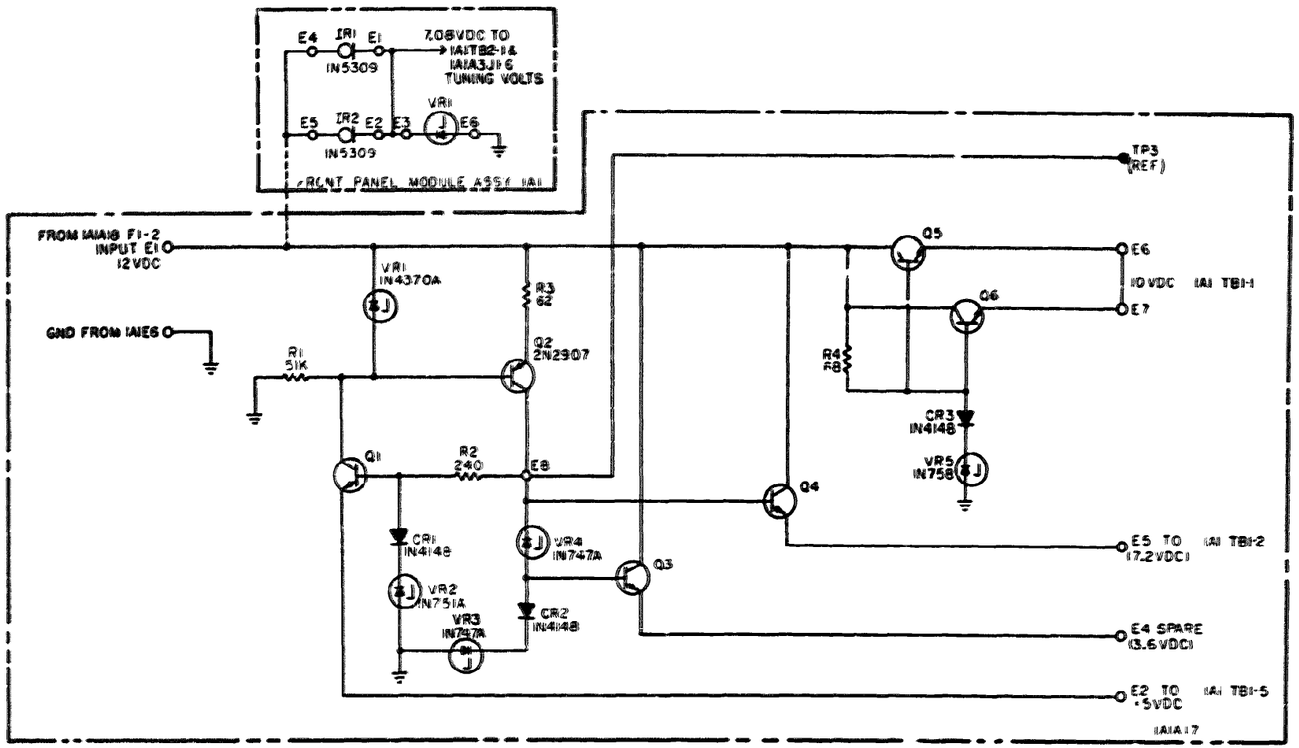



Figure 6-18. Shift register (1A1A15), schematic diagram.




NOTES:
UNLESS OTHERWISE SPECIFIED
1. PARTIAL REFRENCE DESIGNATIONS ARE SHOWN FOR COMPLETE REFERENCE DESIGNATION PREFIX WITH UNIT NO AND SUB ASSY DESIGNATION 1A1A17
2. RESISTORS ARE IN OHMS 1/4W ±5%
3. ALL TRANSISTORS ARE 2N1481

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Figure 6-19. Power supply regulator (1A1A17), schematic diagram.

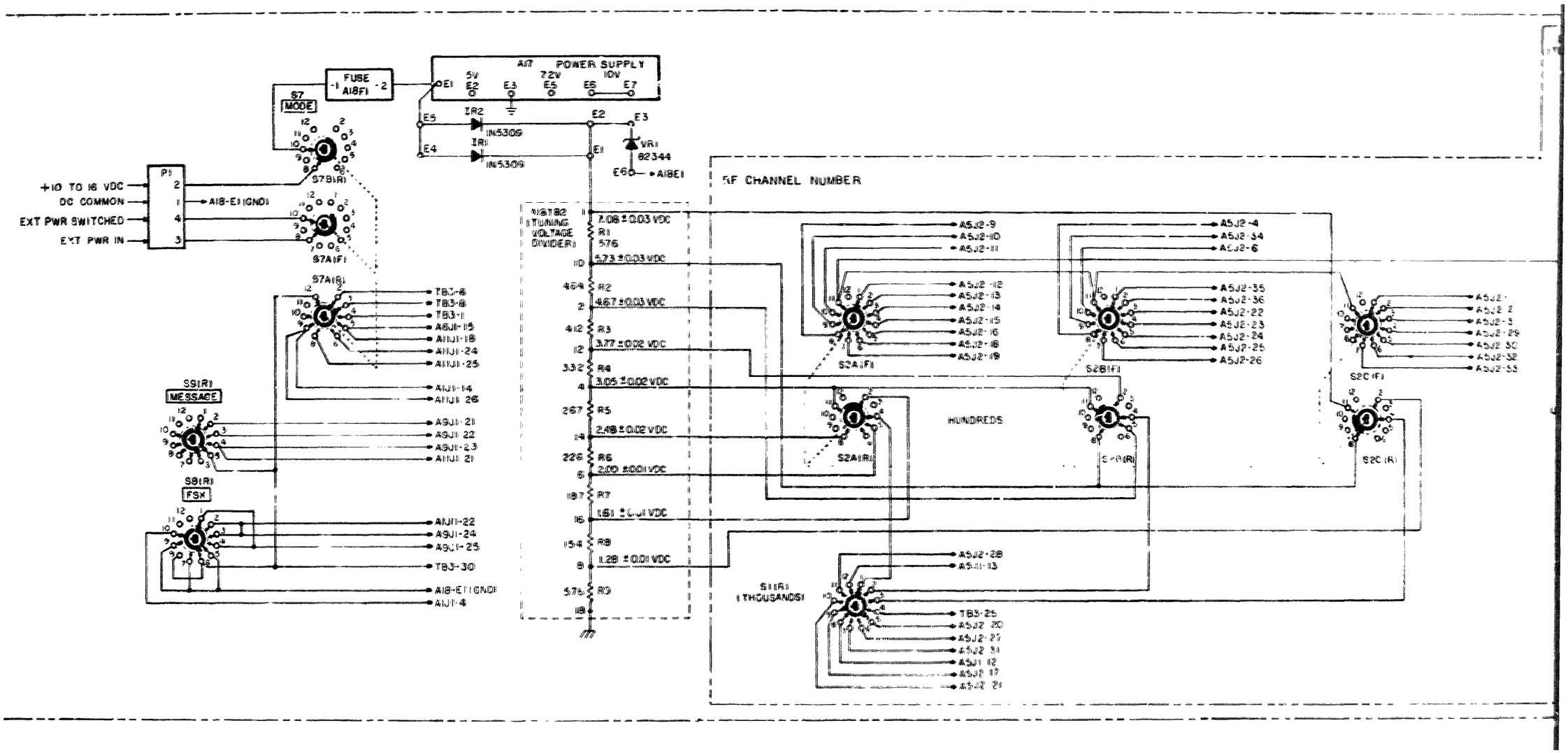
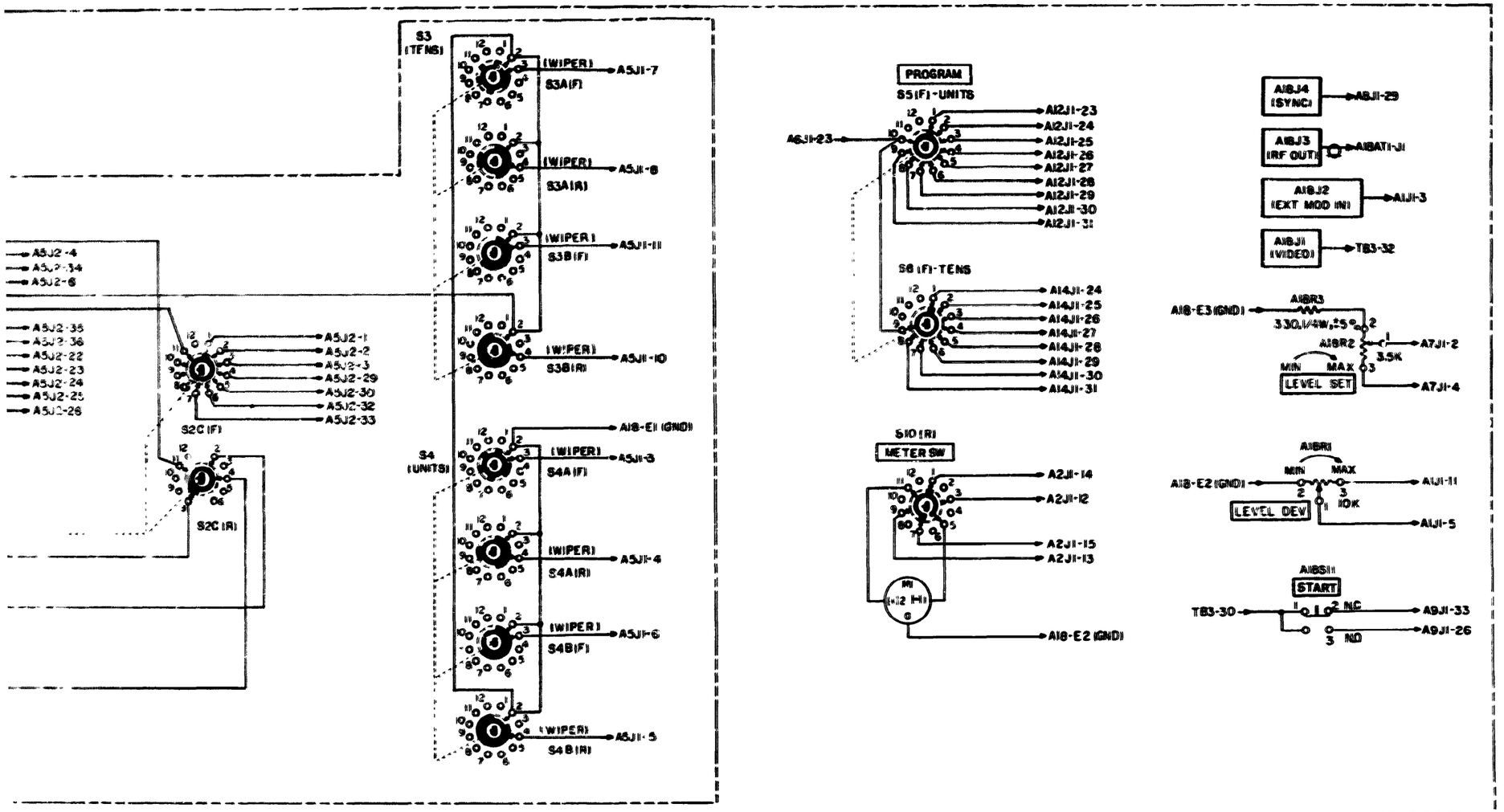



Figure 6-20. Front panel control interface (1A1A18), schematic diagram.




NOTES:
UNLESS OTHERWISE SPECIFIED
1. RESISTOR VALUES ARE IN OHMS, 1/8W, ±1%
2. SWITCHES ARE DRAWN AS IF VIEWED THROUGH THE FRONT PANEL ASSEMBLY (A1A18. ALL SWITCH POSITIONS CORRESPOND TO THEIR EXTREME COUNTCLOCKWISE POSITION (I.E., S7A(R) IS IN SEG A MODE).

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Figure 6-20. Front panel control interface (1A1A18), schematic diagram.

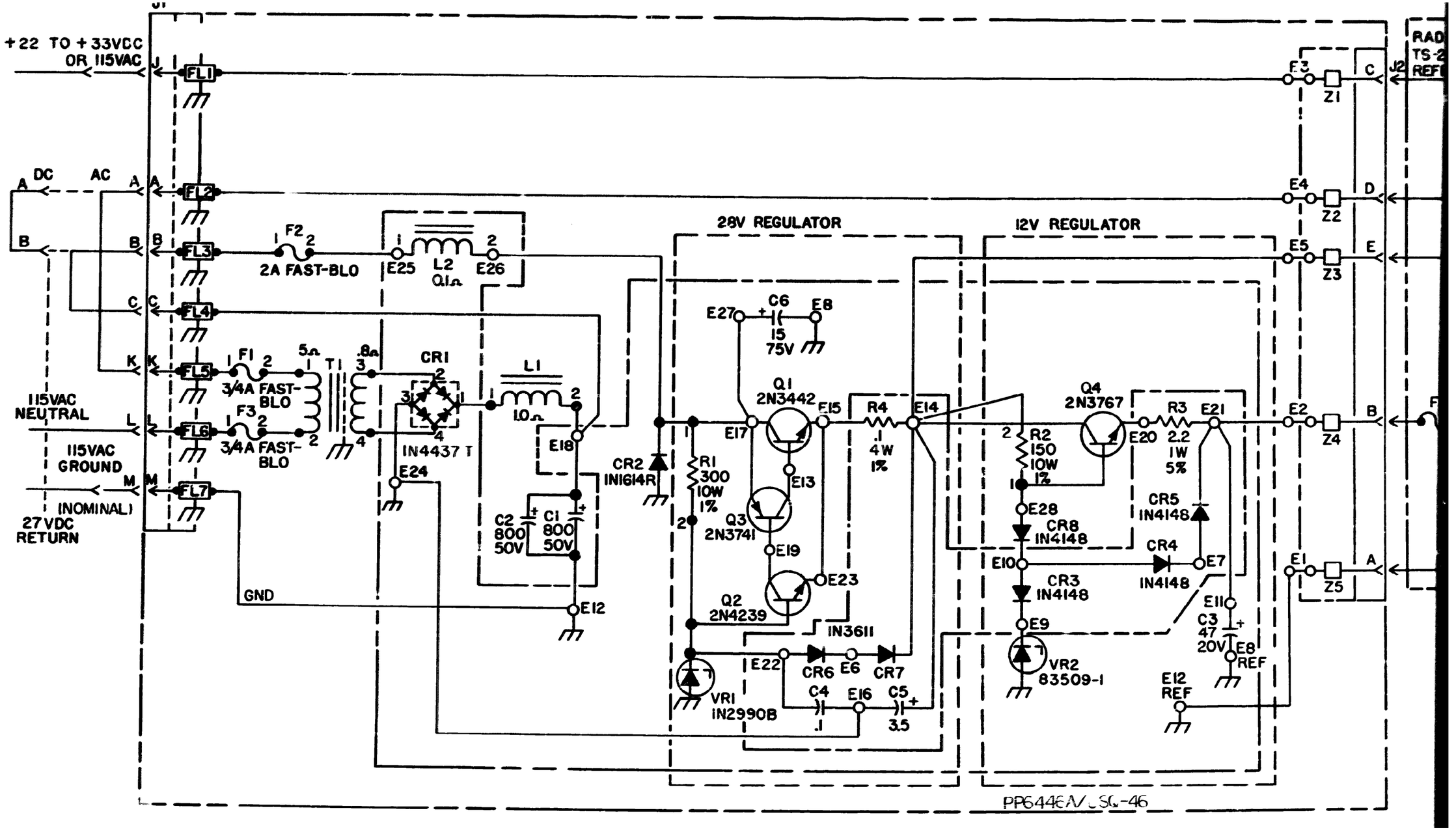
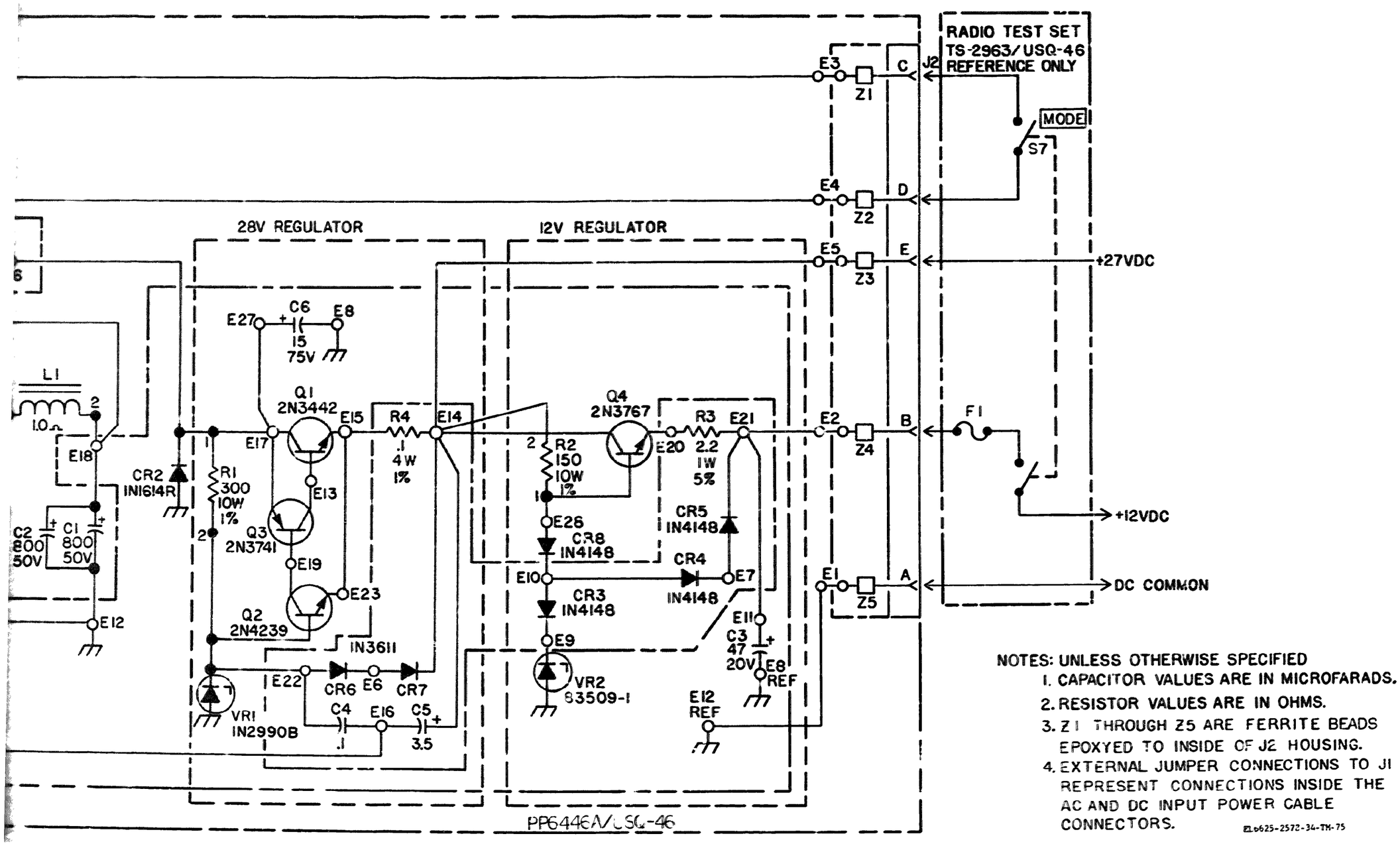



Figure 6-21. Power supply PP-6446A (1A2), schematic diagram.




NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITOR VALUES ARE IN MICROFARADS.
2. RESISTOR VALUES ARE IN OHMS.
3. Z1 THROUGH Z5 ARE FERRITE BEADS EPOXYED TO INSIDE OF J2 HOUSING.
4. EXTERNAL JUMPER CONNECTIONS TO J1 REPRESENT CONNECTIONS INSIDE THE AC AND DC INPUT POWER CABLE CONNECTORS.

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Figure 6-21. Power supply PP-6446A (1A2), schematic diagram.

ALPHABETICAL

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**CREIGHTON W. ABRAMS**
*General, United States Army*
*Chief of Staff*

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**VERNE L. BOWERS**
*Major General, United States Army*
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**USACDCCEA**
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**USAERDAW (2)**
**Sig FLDMS (2)**
**USARV (5)**
**Gen Dep (5)**
**Sig Dep (12)**
**Sig Sec Gen Dep (8)**
**8th Eighth (10)**

*NG:* None.

*USAR:* None.

**For explanation of abbreviations used, see AR 310-50.**

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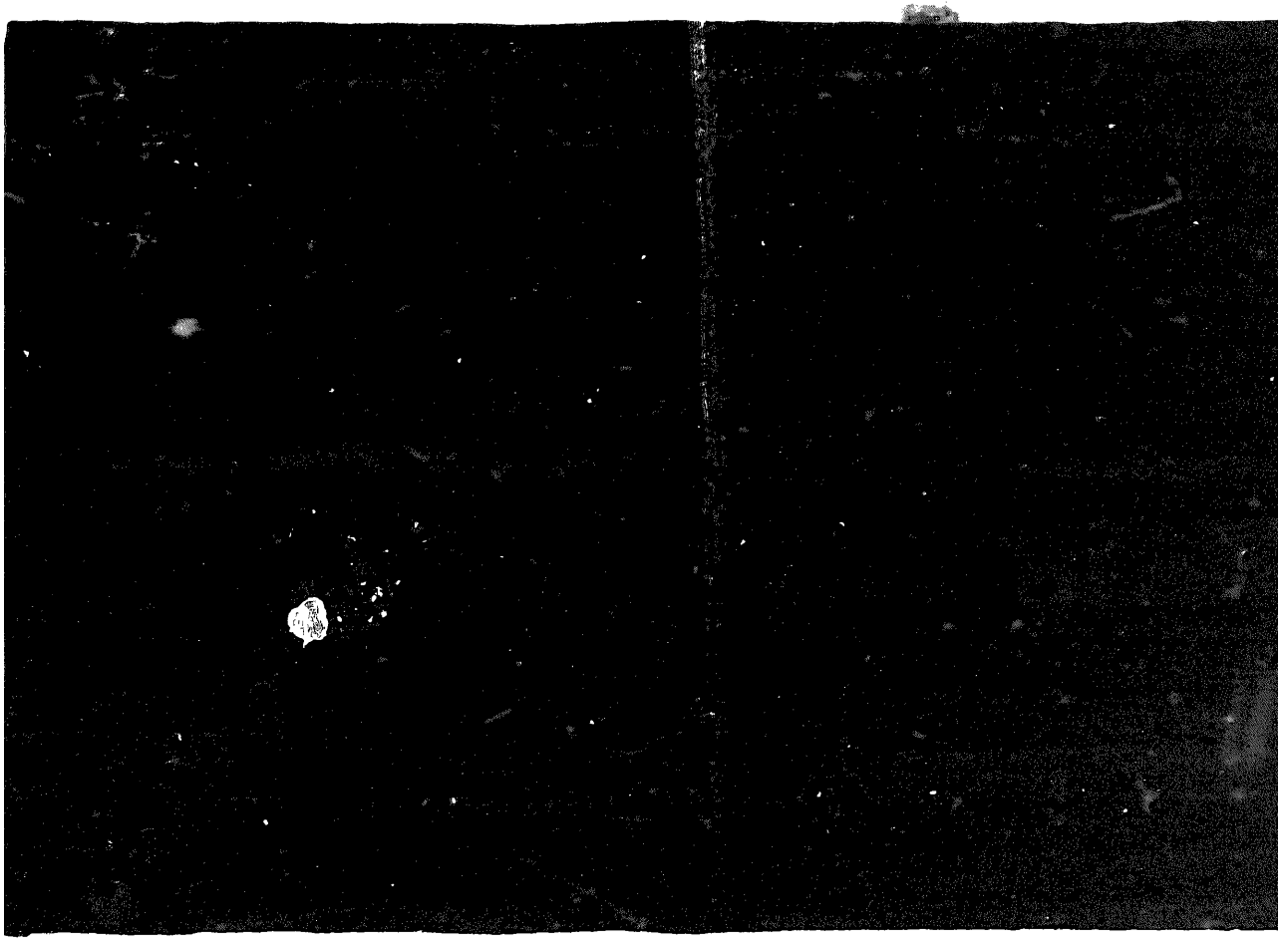
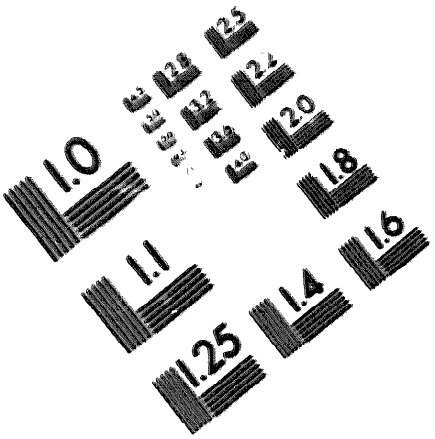
9-18-83

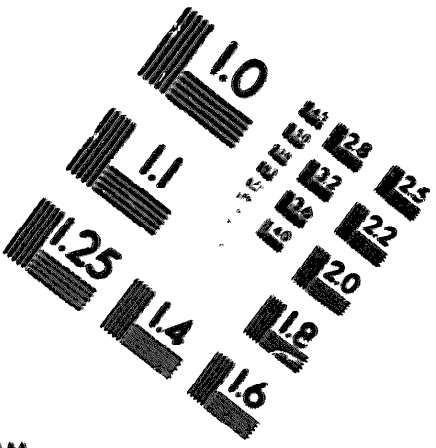
DATE



DEPARTMENT OF THE ARMY

MICROFORM
TEST TARGET




150 MM

1.5 mm (e= 1.09 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

2.0 mm (e= 1.37 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*

2.5 mm (e= 1.77 mm)

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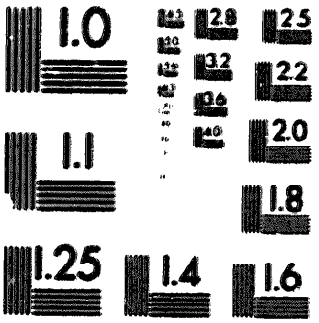
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*




1.5 mm (e= 1.09 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

2.0 mm (e= 1.37 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*

2.5 mm (e= 1.77 mm)

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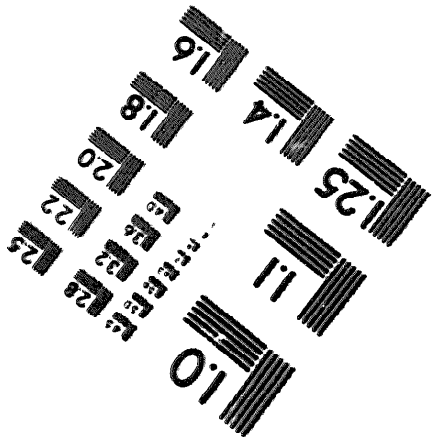
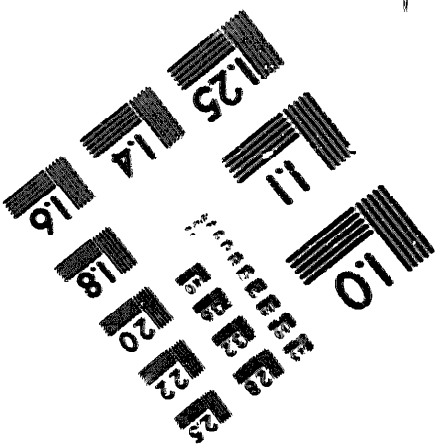
200 MM




250 MM